AGP

INSTRUCTION MANUAL

750EM M557

BOEING P/N 63-11956

Ectron
CORPORATION

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SECTION I

750EM M557 Amplifier

DESCRIPTION

The 750EM-M557 is a true differential amplifier featuring state-of-the-art technology. In addition to providing high common mode rejection and low pumpout current, the following unique features are provided:

1. Simultaneous wide band and filter outputs are available.

2. Internal contact closures provide gain and filter switch status.

3. An internal jumper can be installed in one of two positions to provide amplifier configuration ID.

4. An overload condition sets a latch which must be cleared by an external dc level. A front panel indicator is illuminated during overload periods. An output also is provided showing the status of the overload indicator.

5. An external dc level operates a calibration relay which is located at the input to the amplifier. The relay, when activated, connects a 40:1 divider across the input to the amplifier.

All input signals, control levels, and ac power are applied to a 44 pin double readout card edge connector located at the rear of the amplifier case. The front panel is removeable to reveal another panel screened for different amplifier configurations. The gain and filter switches, zero controls, gain vernier, overload indicator and locking screw are located on the front panel. The exterior case consists of aluminum side panels and top and bottom extrusions.

The gain steps and filter frequencies are available in two configurations. The -5 configuration has standard gains in a 1, 2, 5 sequence to 1000 and filter corner frequencies in a 1, 3, 10 sequence to 10000 Hz and wide band. The -6 configuration has fractional gains and filter corner frequencies. The configurations are easily replaceable in the field, and the position of an internal jumper provides identification of the configuration. Two panels are superimposed on the front of the amplifier and are positioned so that the silk screening on the visible panel conforms to the internal configuration.

Isolation of RFI interference is accomplished by using filters or isolators on all external digital lines.

The enclosures are available in three different configurations. The -2 enclosure has mating connectors installed for the card edge connector on ten amplifiers. No wiring is included in this configuration. The -3 and -4 enclosures have the same mating connectors as the -2, but wiring is included for external signal input connectors, amplifier output and monitor/calibration connectors. The -3 configuration enclosure accommodates ten amplifiers and the -4 accommodates four amplifiers.

SECTION II

SPECIFICATIONS

750EM-M557 Amplifier

Input

Impedance

Resistive (non-overload condition)	>10 M ohms
Overload, 20V maximum	>1 K ohm
Capacitive (includes enclosure wiring)	<500 pf

Pumpout	<5 na over temperature range

Calibration

1	Accuracy	± 0.003%
2	Temperature Coefficient	<2 ppm/degree C
3	Input Resistance	20K ohms ± .1%

Gain (Vernier Switch out)

Range,	-5	0*,1,2,5 to 1000 in a 1, 2, 5 sequence
	-6	0*,20.35,30.52,43.6, 61.04, 101.73,152.58, 203.45, 305.17,435.96, 610.35

*In this position, the gain of the amplifier to input signals is zero, however, the gain of the amplifier to calibration signals is one.

Accuracy (Vernier Switch Out)	±0.1%
Vernier	10% overlap

Stability

24 hours	<±0.01%
6 months	<±0.1%
Temperature Coefficient	<0.005%/degree C

Common Mode

Rejection (40KHz Measurement Bandwidth)	Conditions
>60db + A*	dc to 100Hz Common Mode Voltage 0 to 20V peak 0 to 1K ohm unbalance
>60db + A - 20 Log $\left(\frac{F}{100}\right)$*	100Hz to 1KHz Common Mode Voltage 0 to 20V peak 0 to 1 K ohm unbalance
>60db + A - 20 Log $\left(\frac{F}{100}\right)$*	1KHz to 20KHz Common Mode Voltage 0 to $\left[20\ \frac{(1KHz)}{F}\right]$ V peak 0 to 1 K ohm unbalance
>60db + A - 20 Log $\left(\frac{F}{100}\right)$*	20KHz to 100KHz Common Mode Voltage 0 to 1V peak 0 to 1 K ohm unbalance

*A = Gain of Amplifier
*F = Frequency of common mode signal

Output Offset Due to Common Mode Voltage

Max. Offset	Conditions
$\pm$ 2 mv	dc to 100Hz Common Mode Voltage 0 to 20V peak 0 to 1 K ohm unbalance
$\pm$2 mv	100Hz to 10KHz Common Mode Voltage 0 to 10V peak 0 to 1K ohm unbalance
$\pm$2 mv	10KHz to 100KHz Common Mode Voltage 0 to 1V peak 0 to 1K ohm unbalance
CMV where CMV is the peak value of the common mode voltage	100KHz to 100MHz Common Mode Voltage 0 to 1V peak

Linearity <±0.01% FS

Outputs

Volts	>+ 10.0
Maximum Current	>80, <100mA
Linearity	±1%
Impedance	<0.2 ohms, dc to 40KHz
Capacity Load	<0.22mf without instability
Short Circuit	No damage
Isolation from power lines	>100 M ohms <100na current

Maximum current both outputs simultaneously is 110mA

Recovery	Conditions
<200uS to ±1mv	Input signal up to full scale step
<200uS to ±5mv	Input signal up to 5 times full scale step
<10ms to ±5mv	Input signal from 5 times full scale to ±20v

Noise -5 (Specifications in volts p-p)

dc to 50KHz	19uV RTI + 1mV RTO
dc to 10KHz	10uV RTI + 0.6mV RTO
dc to 1KHz	6uV RTI + 0.4mV RTO
dc to 100Hz	3uV RTI + 0.3mV RTO
dc to 10Hz	1uV RTI + 0.2mV RTO

Noise -6

dc to 256 Hz	4uV RTI + 0.4mV RTO
dc to 128 Hz	3uV RTI + 0.3uV RTO
dc to 64 Hz	2uV p-p + 0.2mV RTO
dc to 16 Hz	1uV p-p + 0.2mV RTO

Response

Wideband	-3db to >40KHz
Filtered (-5)	-3db at 1,3,10,30,100,300Hz 1KHz, 3KHz, 10KHz
Filtered (-6)	-7.6db at 1/8,1/4,1/2,1,2,4, 8,16,32,64,128,256 Hz

Interchangeability Better than 3%

Environment

Operating	0 - 50 degrees C
Storage	-30 to +85 degrees C
Humidity	10 - 90%

Power

Voltage	117 ±10 Vac
Frequency	50 - 420Hz
Current (nominal)	60mA, no load

Weight

(per amplifier)	6.5 lbs. (2.96 Kg.)

SECTION III

THEORY OF OPERATION (DWG 750-613)

General

The 750EM-M557 is a state of the art differential amplifier having several unique features. For example, the zero position on the front panel gain switch places a short on the inputs to the amplifier without placing a short on the signal inputs. Separate wafers on the gain and filter switch provide status ID and isolation is accomplished by reed relays. An external 24V dc applied to the card edge connectors 27 and 28 actuate a relay which connects a precision 40:1 divider to the amplifier input. Amplifier configuration ID is accomplished by placing an internal jumper in one of two positions. A comparator senses an overload condition. When this occurs, an associated logic circuit illuminates a front panel LED and provides an external signal. An external level applied to 17 and 19 resets the logic through an optical isolator. Simultaneous wideband and filter outputs are available and are unique as they provide ±1% linearity to 80mA but less than 100mA under short circuit conditions. The power supply is conventional. Connections are made to the amplifier by a 44 pin double readout card edge connector. The right (component) side is identified by odd numbers. Please refer to Dwg. 750-613 and figures 3-1 through 3-6 for the following discussion.

Input and Calibration Circuits

Figure 3.2 is a simplified schematic of the signal input and relay switching circuits. The input signals are applied to 39 and 41 and connect to the bases of Q3. When the gain switch is adjusted to the gain = 0 position, S1-C places a short on the bases of Q3 and opens one signal input lead. The amplifier has a gain of 1 in this position. The signal inputs are clamped to ± 12 volts to prevent damage to Q3.

The inputs to the amplifier can be switched from normal operation and connected to a precision internal divider consisting of R3, 4 and 5. R4 permits adjusting the division exactly to 40:1. The 24 volt relay K1 must be energized for this function.

Gain Switching (Dwg 750-613)

The collectors of Q3 are connected to the gain determining resistors through two inverting amplifiers U2 and U3. The non-inverting inputs of U2 and U3 are held at a dc level of

approximately 14 volts to equal the collector voltages of Q3. The outputs of U2 and U3 connect to the gain determining resistors R1 - R11 of Assy 750-538-01 in the case of a -5 configuration or R1 - R11 and R58 of Assy 750-538-02 in the case of a -6 configuration.

S1-A and S1-B are used to connect the appropriate shunting resistor in the gain divider network to feed back the appropriately reduced signal. S1-C is active only when the gain switch is in the 0 position. In the gain=0 position, S1-C places a short across the input to the amplifier and opens the signal input terminals. S1-D is used as a shield between digital levels on S1-E,F,G,H and the analog circuits.

Bridge Amplifier

Advantage is taken of the inherent common mode rejection capabilities of the bridge amplifier U4. The outputs of U2 and U3 are connected to the inputs of U4 by means of a x0.6 divider consisting of R33, R38 and R42, R43. The average common mode voltage is sensed at the junction of R34 and R41 and is applied to the inverting input of U4. The inverted output of U4 is connected to the wiper R39 and opposes any CMV from the outputs of U2 and U3.

R39 is the dc CMR adjustment. The output from U5-6 is applied to the non-inverting input pin 3 of U5 through U6 which serves to invert the analog signal. A vernier switch S1-A connected to U6-2 selects the front panel potentiometer R47 for variable gain or a resistor R45 for fixed gain. In addition, Section S1-B provides vernier status ID.

Output Amplifiers (Dwg. 750-613)

The output of U5 is connected to the comparator and the wideband output amplifier. There are two identical output amplifiers; one for the wideband output and one for the filtered output.

The output of the bridge amplifier at U5-6 is connected to the non-inverting input of U13. The output of U13 is connected to the base of Q7 through diode CR23. The output of U13 will measure approximately +1.2 volts in respect to output low under no signal conditions due to the forward conduction of CR23 and the b-e drop of Q7.

Q13 is a constant current source. The voltage drop across diodes CR24 and CR25 provide the correct drive to the base of Q12, and also allows the current limiting transistors Q8, 9, 10 and 11 to follow the signal. and 11 to follow the signal.

Transistor Q6 is a constant current source for the negative current limiting adjustment potentiometer R71 and transistor Q14 is a constant current source for the positive current limiting adjustment potentiometer R70. Transistors Q8 and Q10 do not conduct if the output current demand is less than 80mA. If the output current exceeds 80mA, the voltage drop across the current sensing resistors R69 and R72 increases and causes Q8 and Q10 to conduct. Q8 conducts on positive overloads. If either Q8 and Q10 conduct, the base drive is decreased on the output transistors Q7 or Q12 which limits the output current. The gain of the output amplifier is +1.

Comparator

The function of the comparator is to activate the internal logic whenever an overload condition of either polarity exists.

The dual comparator consists of U7 and associated components. The two outputs of the comparator, U7-1 and U7-7, consist of NPN transistors with the emitter connected to -15 and open collector outputs. The output transistors are not conducting in the absence of an overload signal as a zenered 6.2 volts is applied to the inputs. When an overload signal occurs, one of the output transistors will conduct which enables the optical isolator U2 and activates the logic. R58 adjusts the threshold for positive overloads and R55 the negative.

Overload Logic

An overload signal from the comparator sets the latch U1-a and U1-b and activates the monostable multivibrator U3. Under no overload conditions and assuming a reset signal has been applied to the optical isolator U4, the latch U1 is reset and U3-1 and U3-3 are high. As both inputs to U1-c are high, no drive is supplied to the bases of Q10 and Q11; the front panel LED is not illuminated, and no overload condition indication appears at #23 on the card edge connector. In addition, U1-3 is low and there is no base drive to Q12, and no latch indication appears at 21# on the card edge connector.

When the positive or negative comparator changes state due to an overload condition, pin 3 on the optical isolator is connected to -15 volts. Conduction occurs from pin 5 to 6 on U2, and U3-3, U1-a1 are low. U1-3 is high, base drive is applied to Q12, and a latch indication appears at the card edge connector pin #21. When U3-3 goes low, U3-1 also goes low and stays low for 100ms as determined by R23 and C36.

Base drive is applied to Q10 and 11. The front panel LED is illuminated, an overload condition appears at pin 23 on the card edge connector. The latch remains set until a reset is applied to the optical isolator U4.

Filter

Twelve filter positions are selectable by a front panel switch which also provides filter status ID. The filter characteristics are a 2 pole butterworth for the -5 configuration and a four pole bessel for the -6.

-5 Configuration

The gain of the filter is +1. When the filter switch is in one of the three wideband positions in the -5 configuration, the signal passes through U1 unchanged. In this configuration, the filter switch selects the appropriate resistors and capacitors for the 1, 3, 10 and 30 Hz position. Q1 and Q2 are conducting in these positions. The same resistors and capacitors are used for the 100, 300, 1000 and 3000 position, but the corresponding positions in S2-c apply a negative voltage to the gates of Q1 and Q2 removing C2 and C4 from the circuit. Separate resistors are used for the 10 KHz position, and Q1 and Q2 remain out of the circuit.

-6 Configuration

Twelve filter frequencies are selectable by the front panel switch S2. The gain of the fiter output amplifier is also +1. The -6 configuration is somewhat different than the -5 configuration in that S2 selects four resistors for each position. Figure 3-6 is a simplified schematic. FET's Q1-Q4 conduct at frequencies 1 Hz and below, which parallels capacitors for the lower frequencies. In the 2 and 4 Hz positions, S2-A and S2-B uses the same resistors as are used in the 1/2 and 1 Hz position, however, S2-E holds the FET's Q1-Q4 in the off condition, which enables the higher frequencies. All contacts on S2-F are grounded, and act as a shield between the analog and digital sections of S2.

Power Supplies (Dwg. 750-613)

Four secondaries on the power transformer T1 supply power for al circuits in the amplifier.

Sec.1 with U8, U9 provide floating $\pm$ 18 volts regulated for all analog circuits before the bridge amplifier U5.

Sec.2 provides $\pm$ 32 volts unregulated for the Common Mode Amplifier U1.

Sec.3 is a multi-tapped winding which supplies the following:

a. ± 20 volts unregulated for the limiting transistors Q8-11 and Q17-20 in the output amplifiers.

b. ± 14 volts unregulated for the output amplifiers.

c. ± 15 volts regulated for the comparator U7 and the coils in the reed relay switches, and for output related op-amps.

d. - 23 volts unregulated for Q1, Q2 on the filter. The circuit is a voltage doubler.

Sec.4 supplies 5V regulated for the overload logic.

Common Mode Amplifier (Dwg. 750-613, Fig. 3-3)

If the center tap of the transformer secondary S1 which provides a ± 18 volts to the input amplifiers were connected to output low which is conventional, then the maximum permissibe common mode voltage would have to be less than ± 18 volts to avoid destroying Q3. The maximum common mode voltage specification, however, is ± 20 volts.

The amplifier employs a unique circuit to allow ± 20 volts common mode voltage without damage to the input circuit. This is done by using a floating power supply for the input stages, and driving the common of the floating supply with a common mode amplifier. In this manner, the ± 18 volt supplies for the input amplifiers are referenced to output low with the common mode voltage.

Figure 3-3 is a simplified schematic of the input circuit, bridge amplifier and power supply. The average of the common mode voltage appears at the junction of R6 and R7 and is applied to the gate of Q1. The gain of the common mode amplifier is +1, and the common mode voltage appears at U1-6. U1-6 is connected to the center tap of secondary S2 is connected to output low.

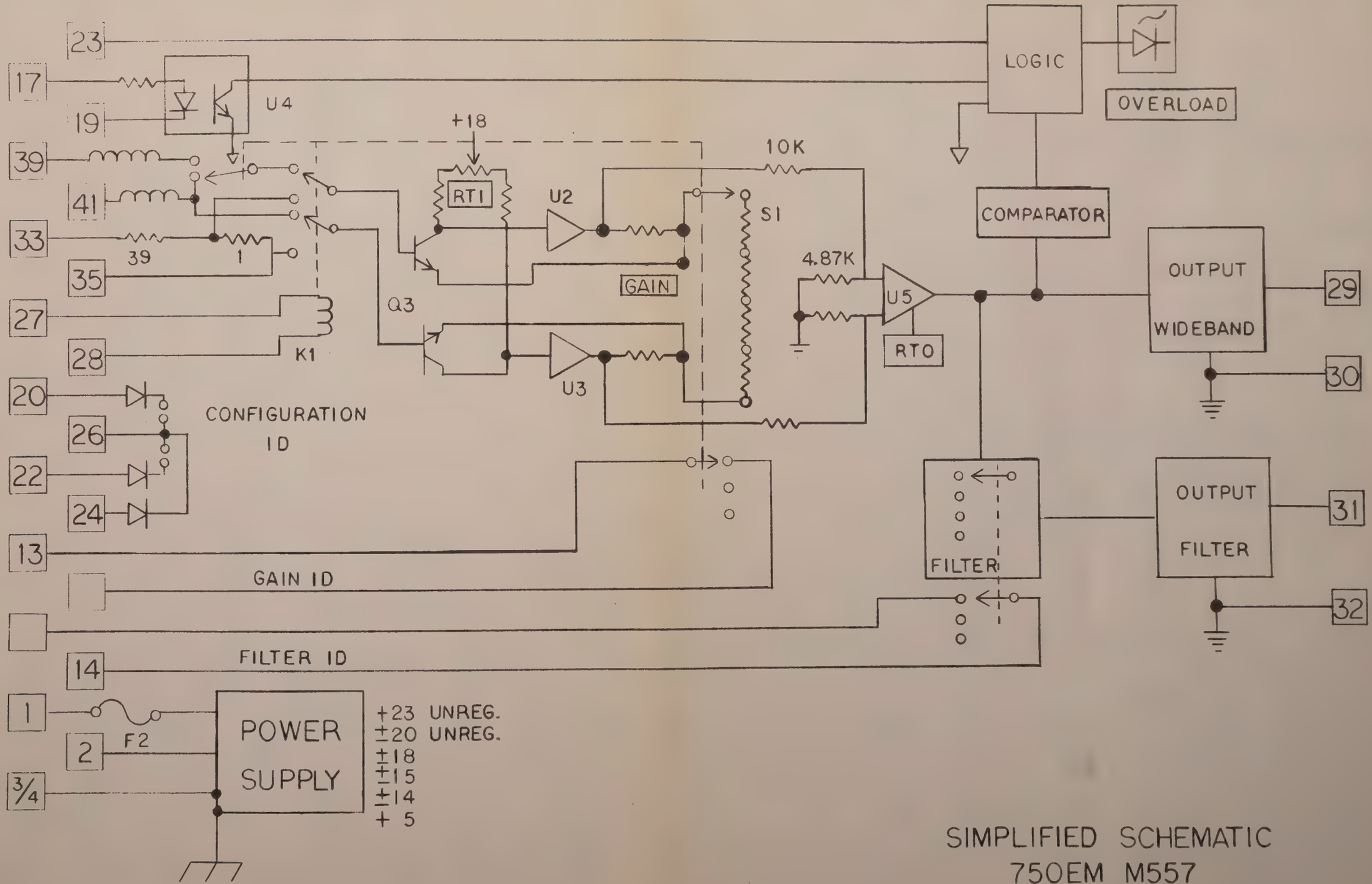
In the absence of any common mode voltage, there is little voltage between floating common at U1-6 and output low.

Assuming a +5 volt common mode voltage is present, the floating common will also have +5 volts in respect to output low. The ±V cc voltages will measure +23 and -13 volts in respect to output low, however, the ± V cc voltages for Q3,

U2 and U3 will still measure ± 18 volts in respect to the center tap of S1. The common mode voltage also appears at the outputs of U2 and U3 and is divided by three and connected to the inputs of the bridge amplifier U5. U4 senses the average common mode voltage at the outputs of U2 and U3 and drives the inputs to U5. The inherent common mode rejection capability of U5 removes the remaining common mode voltage. R39 is used to balance the inputs to U5 for maximum common mode rejection.

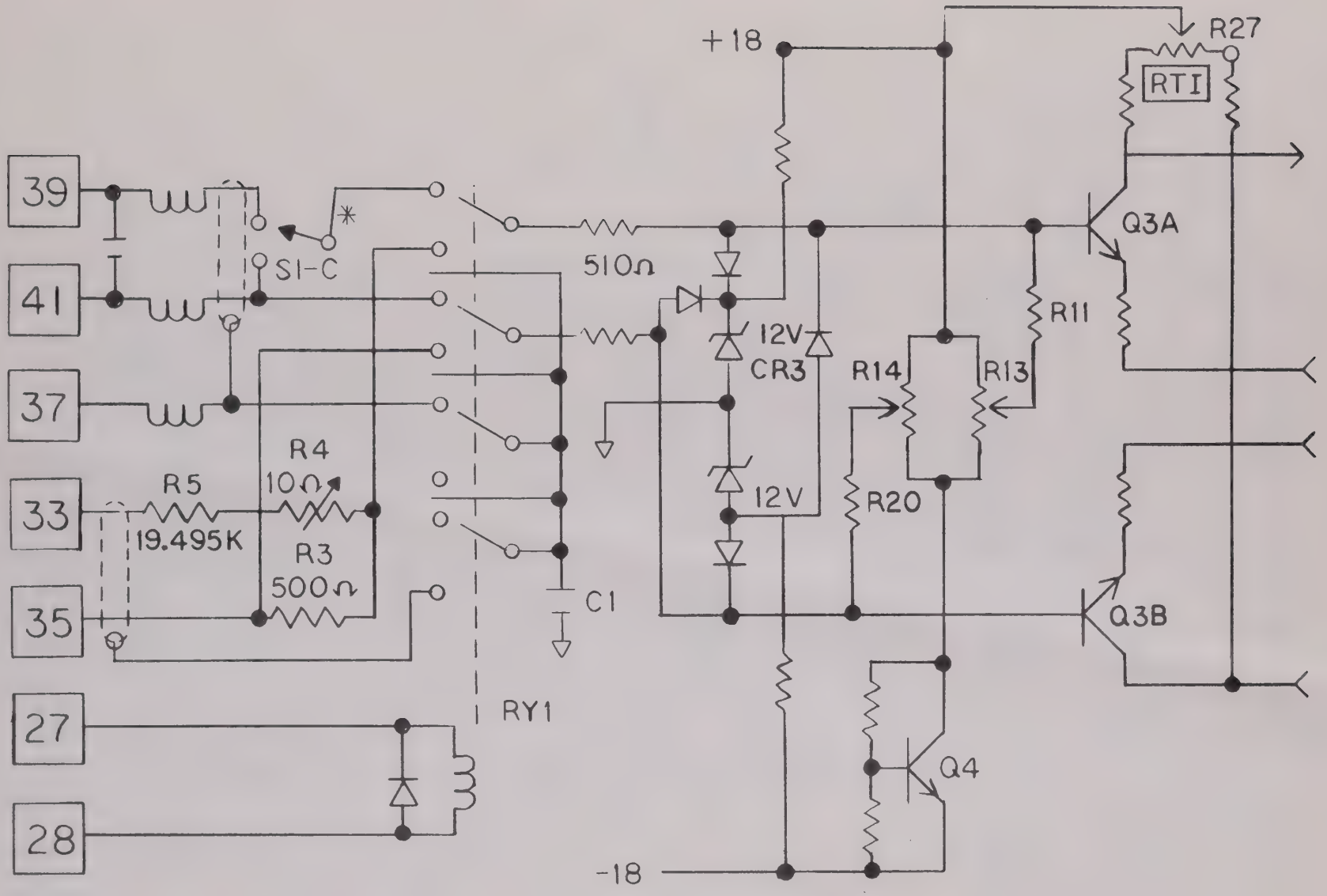
Gain, Filter and Vernier Status

The four rear wafers on the gain and filter switch provide binary information for status ID, and one section of the vernier in-out switch is used to provide vernier status ID. Isolation is obtained by using reed relay switches. In addition, transistors operate the reed relays to further increase isolation.



SIMPLIFIED SCHEMATIC
750EM M557

FIG. 3-1

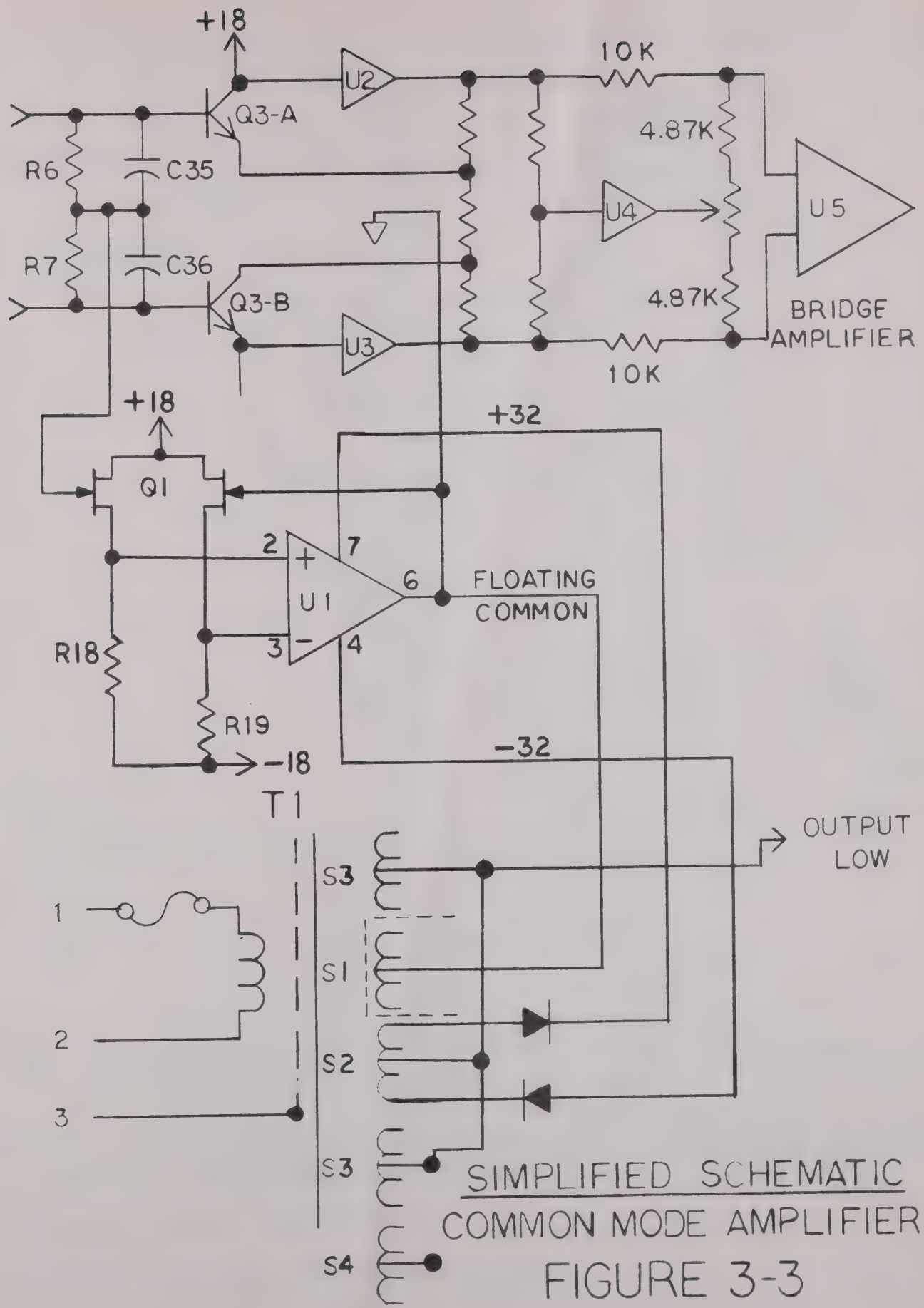


*SI-C IS SHOWN NOT IN GAIN = 0 POSITION.

SIMPLIFIED SCHEMATIC

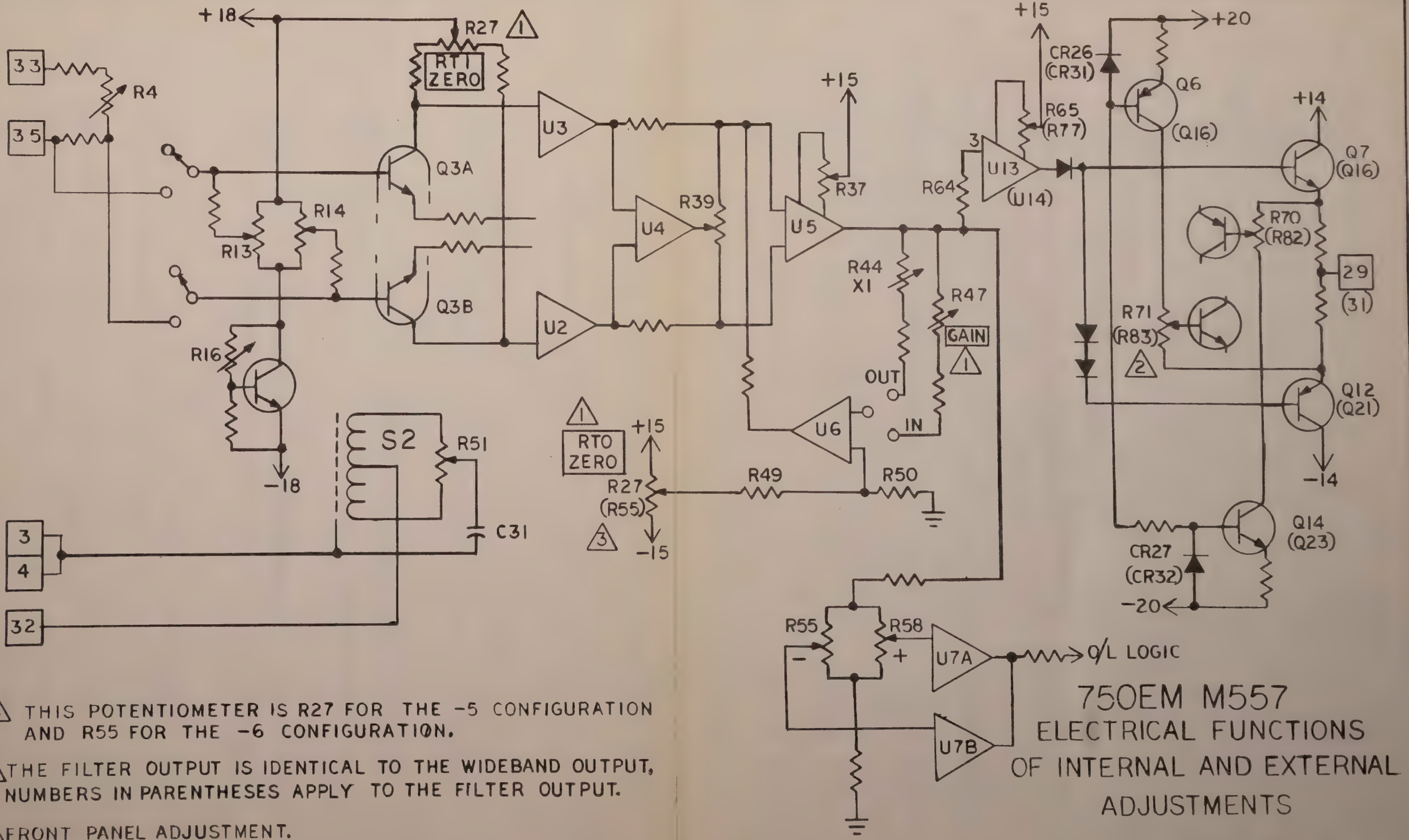
750EM M557 INPUT AND CALIBRATION

FIGURE 3-2



SIMPLIFIED SCHEMATIC
COMMON MODE AMPLIFIER

FIGURE 3-3



3 THIS POTENTIOMETER IS R27 FOR THE -5 CONFIGURATION AND R55 FOR THE -6 CONFIGURATION.

2 THE FILTER OUTPUT IS IDENTICAL TO THE WIDEBAND OUTPUT, NUMBERS IN PARENTHESES APPLY TO THE FILTER OUTPUT.

1 FRONT PANEL ADJUSTMENT.

NOTE UNLESS OTHERWISE SPECIFIED

750EM M557
ELECTRICAL FUNCTIONS OF INTERNAL AND EXTERNAL ADJUSTMENTS

FIGURE 3-4

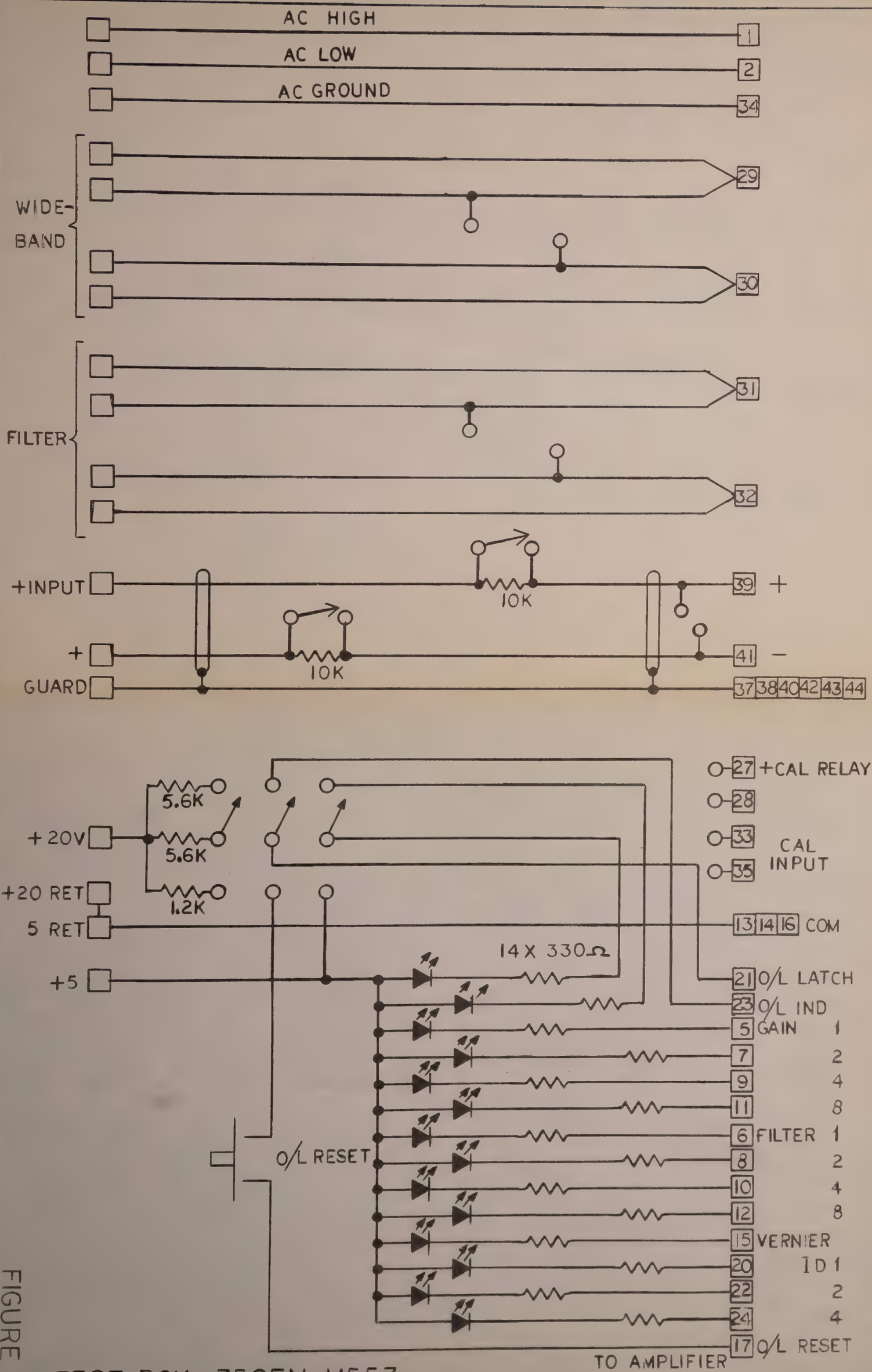
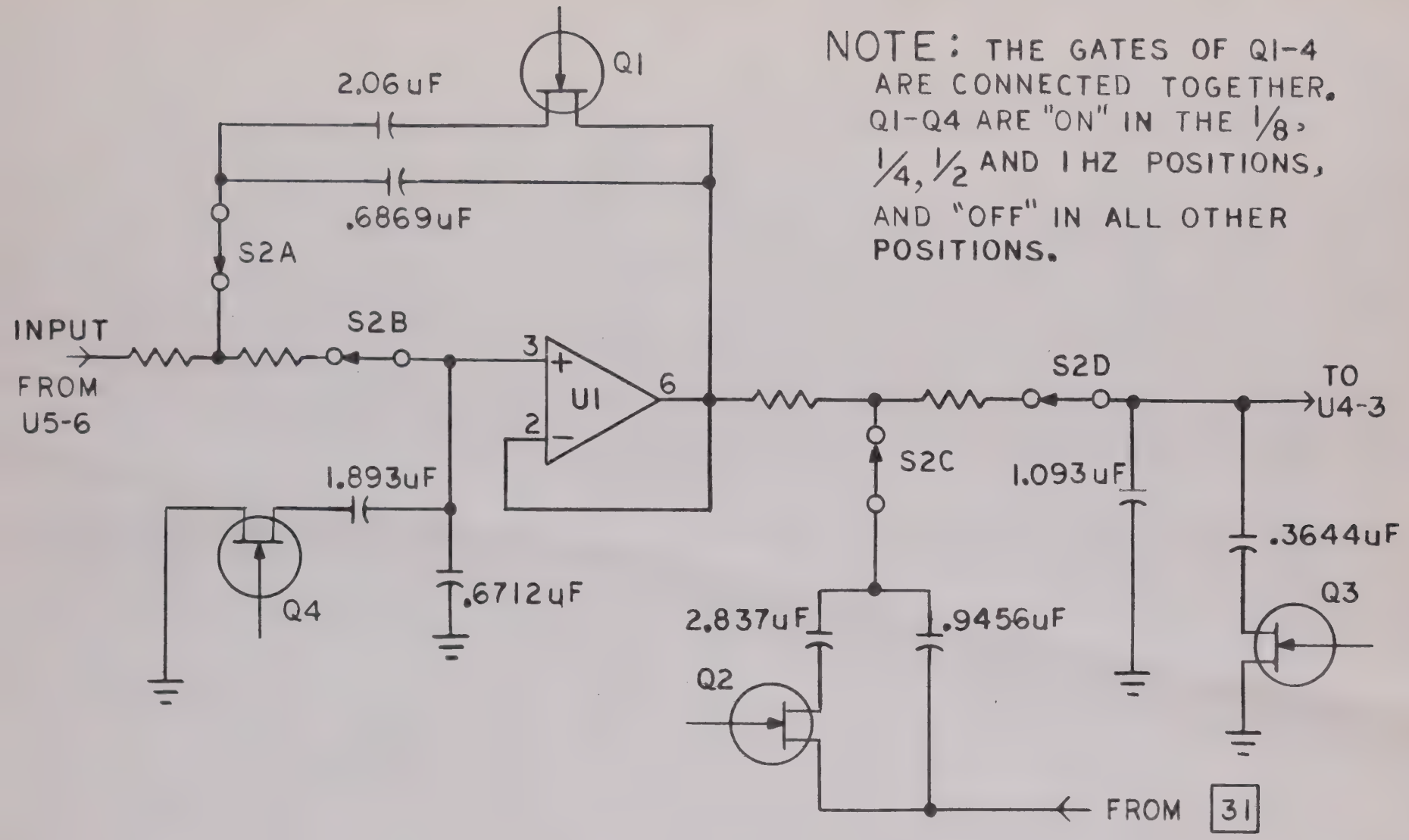


FIGURE 3-5

TEST BOX 750EM M557

090-627 REV A



750 M557

SIMPLIFIED SCHEMATIC
OF -6 FILTER
750-538-02

FIGURE 3-6

SECTION IV
MAINTENANCE AND CALIBRATION

General

Drawing 750-613 which appears at the end of this manual is complete for both the -5 and -6 configurations. The amplifier consists of three separate assemblies as follows:

1. Amplifier Assembly 750-536-01.

2. Centerline Assembly 750-537-01.

3a. Switch Assembly - 5 configuration 750-538-01.

3b. Switch Assembly - 6 configuration 750-538-02.

The Amplifier assembly is the large board containing the power transformer, power supplies and the basic amplifier.

Two Switch assemblies are available. One is used for the -5 gain and filter configuration, and the other for the -6 configuration. The Switch assembly is hinged and is readily identified by the two 8 wafer rotary switches. It contains the gain determining resistors, the filter resistors and capacitors.

The Centerline assembly is also hinged and contains the isolated contact closures for external gain and filter ID, the logic for overload indication and provision for jumpers to identify the amplifier configuration. It is readily identified by top and bottom shields.

Note that each assembly has a separate series of reference designators. Q4, for example, appears in three places on Dwg. 750-613.

Many voltage measurements are referenced to output low, pins 30, 32 on the card edge connector. A convenient test point for output low is the negative end of C14 as there are no components close to C14- which might be damaged. Another point is the centerline assembly shield. The floating common is readily accessible at the positive end of C17.

There are no potentially lethal internal voltages in the amplifer except for the primary connections to T1.

CAUTION

Do not jumper the floating common to output low unless U1 has been removed.

Equipment Required

The equipment listed on pages 1 and 2 of the Acceptance Test procedure which appears at the end of this manual should be available for proper maintenance.

Figure 3-5 is a schematic of a test box which is used to facilitate testing and calibration of M557 amplifiers. It is used in addition to a Universal Amplifier test box. The Universal Amplifier test box supplies metered 117 volts ac through a variable transformer, dc and ac common mode voltages, appropriate loads with a four wire configuration and it contains a precision divider for gain calibration. A differential connection is used for all gain measurements.

Power Supplies

The nominal current of a functional amplifier with no load at 117 V ac is 60 mA.

The following table shows the nominal voltages and peak to peak ripple of all internal power supplies. The readings were taken from a serviceable amplifier with the gain at 0 and the line voltage at 117V, 60Hz. Inputs shorted and returned to output low.

Location	Reference	Volts	Ripple p-p
C18+	C18-	32.7	60mV
C19-	"	32.8	100mV
C23-	"	19.4	35mV
C20+	"	19.7	800mV
C21-	"	19.9	800mV
C14+	"	16.4	100mV
C15-	"	16.9	30mV
*C28+	"	15.0	0.5mV
*C29-	"	15.0	0.5mV
*C27+	C26+	18.0	2mV
*C28-	"	18.0	2mV
*C30+	C30-	5.0	1mV
C27-	C14-	0.±100mV	1mV

*Items marked with an asterisk are regulated supplies and should hold regulation to 107 V ac line when the amplifier is operating under full load. A failure in any of the regulated supplies is very likely due to a failure of one of the three terminal regulators U8-U12.

Common Mode Amplifier

The common mode amplifier is a high impedance input amplifier with a gain of +1. It consists of Q1 and U1 on the amplifier assembly.

1. Adjust the function generator for 20 V p p at 100 Hz.

2. Connect the low side of the function generator to C14-.

3. Adjust the gain of the amplifier to 1.

4. Connect the high side of the function generator to the inputs and guard of the amplifier (card edge connectors 39, 41, 43).

Measure the ac voltage at C17+ in respect to C14-. The voltage should also be 20 Vp-p at 60Hz and in phase with the applied signal.

INPUT DUAL NPN, U2 AND U3

5. Position the gain switch to 0.

6. Measure each collector and emitter voltage with a DVM in respect to C17+.

   The collector voltages should be equal and measure +14.2 volts nominally and the emitter voltages should be +0.5V nominally.

7. Position the gain switch to 1.

8. Apply a 200mV p-p 100Hz sine wave to the card edge connector 39 in respect to 41 and 43.

9. Using a differential oscilloscope, measure the signal between U2-6 and U3-6 in respect to C14-.

   The signal should be 200mV p-p and no distortion should be apparent.

Bridge amplifier U5

10. Adjust the oscilloscope for single input and connect the probe to U5-6 and the low side to C14-. Ensure that the vernier switch S1 is in the OUT position.

    The signal at U5-6 should measure 200mV p-p.

    As the wideband output amplifier has a gain of +1, the junction of R69 and R72 should also measure 200 mV p-p.

The filter output amplifier can also be checked in the same manner. The peak to peak voltage at the junction of R81, R84 should also measure 200mV p-p providing the filter switch is in the wide band position.

Gain and Filter ID (Dwg. 750-613)

The four rear wafers on the Gain and Filter switches operate relays which provide isolated contact closures for gain and filter ID in a binary format. The contacts in the wafers apply base drive to Q1 through Q8 which close relays K1 through K8. The BCD common for the gain ID is separate to the common for the filter ID.

The contact closures can be checked with an ohmmeter as follows:

Filter/Gain Position	Card Edge Connector Gain	Filter
1	none	6-14
2	5-13	8-14
3	7-13	6-8-14
4	5-7-13	10-14
5	9-13	6-10-14
6	5-9-13	8-10-14
7	7-9-13	6-8-10-14
8	5-7-9-13	12-14
9	11-13	6-12-14
10	5-11-13	8-12-14
11	7-11-13	6-8-12-14
12	--	10-12-14

If a contact closure is missing, check for approximately 6 volts across the suppressor diode which is connected across the relay. The relay coil is 800 ohms nominally. If 6 volts is present, and the relay contacts are not closing, the relay must be replaced. If 6 volts is not present, the corresponding transistor is not conducting. Ensure that there is base drive to the transistor.

INTERNAL ADJUSTMENTS

Figure 3-4 which was derived from Dwg. 750-613 is a simplified schematic showing the electrical functions of all internal adjustments. It applies to the -5 and -6 amplifier configuration. The effects of the internal adjustments are more readily apparent.

The amplifier must be functional and have passed and the previous tests in this section. Any dc offset will be corrected by the following procedure which must be done in sequence as there is interaction between the adjustments.

Pumpout Current Adjustments

11. Set the amplifier to a gain of 1000.

12. Set the test box gain switch to 0. (This completely shorts the inputs.)

13. Set R16 to midrange.

14. Insert a 10K ohm resistor in the + amplifier input and adjust R13 for minimum pumpout current.

15. Remove the source resistor from the + amplifier input and insert it in the - input. Adjust R14 for minimum pumpout current.

16. R16 may have to be slightly readjusted during temperature.

RTI Zero

17. Electrically center R27.

18. Switch the amplifier gain from 1 to 1000 noting whether the output goes positive or negative.

19. If positive, select a resistor (metal film only) for R28 so that when the gain is switched from 1 to 1000 there is minimum zero shift. NOTE: the output of the amplifier will NOT necessarily be at zero at this time.

20. Recheck the two pumpout adjustments as there may be some interaction with the RTI zero alignment.

COMMON MODE REJECTION ADJUSTMENT AND ALIGNMENT

21. dc common mode adjustment
    a. Set the amplifier to a gain of 10 and the test box to ACCMR with a 100Hz 20Vp-p square wave.
    b. Adjust R39 for minimum square wave out (typically no square wave.)

22. 20KHz common mode alignment
    a. Set the amplifier gain to 1 and the oscillator for a 2Vp-p at 20KHz.
    b. Select a capacitor C9 or C10 to minimize the 20KHz at the output of the amplifier.
    c. Set the amplifier gain to 1000 to observe that the selected value of C9 or C10 is adequate.

23. It may be necessary to change the value of C42 slightly (ceramic caps with stable TC must be used a few times) so that the amplifier will pass the dc offset phase of common mode tests (see test 3.19 of the 2360 ATP) NOTE: C42 also affects high frequency CMR.

GAIN ADJUSTMENT

24. Set the amplifier gain to 1, and the test box to a gain of 1 (internal).

25. Using a +10Vdc signal, adjust R44 for minimum gain error. NOTE: it may be necessary to optimize the adjustment so that all gain steps will be in tolerance.

RTO ZERO.

26. Set the amplifier to a gain of 1 and the test box to a gain of zero.

27. Set the gain vernier pot to maximum CCW.

28. While switching the gain vernier switch in and out, adjust R37 until there is no (less than 0.1mV) difference in the two readings.

29. Adjust R55 for zero out of U5 pin 6.

30. Adjust R65 for zero out of the wide band output.

31. Adjust R77 for zero out of the filtered output.

OVERLOAD INDICATION ADJUSTMENTS

32. At any gain, put in sufficient dc input to obtain +10.25V at the output.

33. Adjust R58 until the overload indicator of the test adapter lights.

34. Obtain -10.25Vdc from the amplifier and adjust R55 for the same.

35. Ensure the light extinguishes before the output goes below + or - 10.0V.

HUM BALANCE ADJUSTMENT

36. Perform test 3.31 of the 2360 ATP and adjust the hum balance pot for the best reading.

CAL CIRCUIT DIVIDER ADJUSTMENT.

37. Perform test 3.8 in the 2360 ATP and adjust R4 for less than 25uV difference.

OUTPUT CURRENT ADJUSTMENTS

38. Obtain +10V from the wide band output, put a current meter across the output, and adjust R70 for 90mA. (or put a 50 ohm load across the output and adjust R70 for 4.5V.)

39. Obtain -10V from the wideband output and adjust R71 for -90mA (-4.5V).

40. Obtain +10V from the filtered output and adjust R82 for 90mA (4.5V).

41. Obtain -10V from the filtered output and adjust R83 for -90mA (-4.5V).

PARTS LIST

750EM M557

The following abbreviations are used for the manufacturers shown.

AB	Allen Bradley
AR	Arco Electronics Inc.
BO	Bourns, Inc.
CD	Cornell Dubilier Electronics
CE	Centralab
CK	C&K Components, Inc.
CL	Clarostat Mfg. Co., Inc.
CR	CP Clare & Co.
EC	Ectron Corporation
EL	Electrocube
ER	Erie Technological Products
FA	Fairchild Camera & Instr.
FE	Ferronics, Inc.
GE	General Electric Co.
GI	General Instruments, Inc.
GY	Grayhill, Inc.
HA	Harris Semiconductors
HP	Hewelett Packard Optoelec.
IR	Inter. Rectifier
JW	J. W. Miller
KE	Union Car., Kemet Division
MO	Motorola
LI	Littlefuse, Inc.
ME	Mepco-electra, Inc.
MI	Micro Ohm, Corp.
MO	Motorola Inc., Comp. Prod.
NA	National Semicond. Corp.
NY	Nytronic Comp. Group, Inc.
PB	AMF Potter & Brumfield Div.
PM	Precision Monolithics, Inc.
RA	Raytheon, Corp.
RO	Rogan
SC	Southco
SO	Solitron
SP	Spectrol
SR	Sprague
TI	Texas Instruments, Inc.
TS	Teledyne Semiconductor

AMPLIFIER ASSY. 750-536-01

Reference Designator	Qty	MFR.	Part Number MFR.	Part Number Ectron
CR4,5,7,8	4	EC		032-001-01
U2-6,13,14	7	NA	LF356N	1-100356-1
U1	1	HA	HA2-2645-5	1-102645-0
U12	1	MO	MC78LO5CG	1-137805-2
U10	1	FA	UA78M15C	1-137815-0
U8	1	MO	MC78L18CG	1-137818-1
U11	1	FA	UA7915UC	1-137915-0
U9	1	MO	MC79L18CG	1-137918-0
U7	1	NA	LM393N	1-140001-0
CR15-19	5	GI	75W02M	1-190075-0
CR26,27,31,32	4	FA	1N751A	1-190751-2
CR22,35	2	MO	1N961B	1-190961-2
CR3,6	2	MO	1N963B	1-190963-2
CR13,14	2	IR	1N823	1-190823-2
CR1,2,33,34	4	MO	1N4002	1-194002-0
CR23-25,28-30	6	FA	1N4148	1-194148-0
CR20,21	2	MO	1N4750	1-194750-0
Q3	1	PM	MAT-01	1-200001-0
Q7,16	2	MO	2N2219	1-202219-0
Q2,4,5,8,11,13, 14,17,20,22,23	11	GE	2N3415	1-203415-1
Q12,21	2	MO	2N2905	1-212905-0
Q6,9,10,15, 18,19	6	FA	2N4248	1-214248-0
Q1	1	SO	2N3956	1-243956-0
L1	1	FE	21-031J	1-308015-0
C3,5,69,70	4	AR	DM5100J	1-400103-0
C13	1	AR	DM5150J	1-400153-0
C66,67	2	AR	DM5200J	1-400203-0
C2	1	AR	DM5470J	1-400473-0
C62,63	2	AR	DM5620J	1-400623-0
C32	1	AR	DM5820J	1-400823-0
C31,34	2	AR	DM5221J	1-402203-0
C36,37,39,41-, 43,45,49,50, 52,54-56,58	14	SR	5GAD10	1-411004-1
C1	1	ER	8121-100X7R0472K	1-414709-0
C11,12,44,57	4	SR	HY550	1-431004-0
C6-8	3	ER	8121-100-651-104M	1-431009-0
C33	1	ME	C280AH/P100K	1-431009-1
C26,27		KE	CSR13F685K2064	1-446800-0
C28-30,35,38, 40,46,48,51 53,59	11	KE	CSR13E156K2049	1-451500-0

C22,23	2	SR	TE1307	1-455000-2
C16-21	6	CD	NLW125-50	1-461250-0
C24-25	2	CD	NLW450-16	1-464500-0
C14,15	2	ME	ET102X025A03	1-471000-0
R50	1	ME	RN55C1000F	6-100100-0
R52,54	2	ME	RN55C4641F	6-101464-0
R38,40	2	ME	RN55C4871F	6-101487-0
R35	1	ME	RN55C4991F	6-101499-0
R17	1	ME	RN55C1692F	6-102169-0
R34,41	2	ME	RN55C2002F	6-102200-0
R30	1	ME	RN55C3322F	6-102332-0
R57	1	ME	RN55C3162F	6-102316-0
R56	1	ME	RN55C4992F	6-102449-0
R49	1	ME	RN55C7502F	6-102750-0
R15	1	ME	RN55C1153F	6-103115-0
R21	1	ME	RN55C1503F	6-103150-0
R31	1	ME	RN55C1623F	6-103162-0
R22,23	2	ME	RN55D2000F	6-110020-0
R48	1	ME	RN55E8871F	6-121887-0
R32,42,45,46	4	ME	RN55E1002F	6-122100-0
R26,29	2	ME	RN55E1003F	6-123100-0
R8,10	2	AB	RC07GF561F	6-170560-0
R53,74,86	3	AB	RC07GF102F	6-171100-0
R9,12	2	AB	RC07GF682F	6-171680-0
R67,75,79,87	4	AB	RC07GF822F	6-171820-0
R61,64,76	3	AB	RC07GF103F	6-172100-0
R66,73				
R66,73,78,85	4	AB	RC07GF153F	6-172150-0
R18,19	2	AB	RC07/GF203F	6-172200-0
R63	1	AB	RC07GF223F	6-172220-0
R68,70	2	AB	RC07GF273F	6-172270-0
R62	1	AB	RC07GF393F	6-172390-0
R59	1	AB	RC07GF224F	6-173220-0
R6,7,11,20,60	5	AB	RC07GF225F	6-175220-0
R69,72,81,84	4	MI	RW70V	6-217502-0
R32	1	AB	RC07GF220F	6-170022-0
R27,44	2	BO	3006P-1-501	6-450500-0
R55,58	2	BO	3006P-1-103	6-452100-0
R77	1	BO	3006P-1-203	6-452200-2
R13,14,16	3	BO	3006P-1-104	6-453100-0
R4	1	SP	64W100	6-490010-0
R39	1	SP	64W201	6-490200-3
R70,7,82,83	4	BO	3386P-1-102	6-491100-2
R37,65	2	BO	3389P-1-203	6-492200-3
R51	1	BO	3389W-1-205	6-494200-0
R47	1	CL	73JA20K	6-510000-0
K1	1	PB	R11-E2-V1.2K	6-600001-0
S1	1	CK	7201AV-2E	7-110006-1
T1	1	EC		750-032-01
R3,5	1	EC		750-033-01

CENTER LINE ASSEMBLY

U1	1	TI	SN74 LS00N	1-117400-1
U3	1		SN74L121N	1-117412-9
CR3-22	20	FA	1N4148	1-194148-0
Q1-12	12	GE	2N3414	1-203414-0
U2,U4	2	HP	6N138	1-280008-0
L5-7	3	NY	MS75101-7	1-308000-0
L8-12	5	JW	9350-32	1-308011-0
C3-18	16	CE	SFT-102	1-308014-0
C40,46	2	AR	DM5101J	1-401003-0
C47,48	2	ER	8121-100X7R0472K	1-414709-0
C24-26	3	SP	TGS10	1-421004-0
C42	1	ER	8121-100X7R0472K	1-414709-0
C20-23	4	SP	TGS10.002	1-412004-0
C50-52,C19	3	ER	8121-100-651-104M	1-431009-0
C36,49,27-35	11	KE	CSR13E156K2049	1-451500-0
F1	1	LI	275.250	2-160250-0
R23	1	ME	RN55C9531F	6-101953-0
R26	1	AB	RC07GF271F	6-170270-0
R28	1	AB	RC07GF681F	6-170680-0
12,14,16 10, 12,14,16,18, 31-33	12	AB	RC07GF102F	6-171100-0
R29,30,35	3	AB	RC07GF222F	6-171220-0
R20	1	AB	RC07GF153F	6-172150-0
R19,21,24, 25,27	5	AB	RC07GF223F	6-172220-0
R22	1	AB	RC07GF273F	6-172270-0
R1,3,5,7,9, 11,13,15,17	9	AB	RC07GF473F	6-172470-0
K1-9	9	CR	925A12C1A	6-600002-0
L2-4	3	EC		750-036-01
T1	1	BO	4259-0003	8-220000-0
R36	1	AB	RC07GF332F	6-171330-0
C53	1	SR	196D334X9035HAI	1-433300-0

SWITCH ASSEMBLY 750-538-01 (-5 Configuration)

CR1,2	2	FA	1N4148	1-194148-0
Q1,2	2	TS	U1897	1-241897-0
C5,6	2	AR	DM5100J	1-400103-0
DS1	1	HP	5082-4655	4-120014-0
R23	1	AB	RC07GF104F	6-173100-0
R22,24	2	AB	RC07GF106F	6-175100-0
R27	1	BO	3006P-1-503	6-452500-0
S1	1	GY	71AY231631-12-S-F	7-100033-0
S2	1	GY	71AY231630-1-11-S	7-100034-0
R28	1	AB	RC07GF103F	6-172100-0
C7	1	AR	DM5220J	1-402203-0
R14,15	1	EC		021-000-01
C1	1	EL	230B	1-421121-0
C3	1	EL	230B	1-422251-0
C2	1	EL	230B	1-441111-0
C4	1	EL	230B	1-44221-0

R20,21	2	ME	RN55C1001F	6-101100-0
R18,19	2	ME	RN55C3321F	6-101332-0
R16,17	2		RN55C1002F	6-102100-0
R12,13	2	ME	RN55C1003F	6-103100-0
R1-11	1	EC		750-034-01
C8	1	AR	DM5101J	1-401003-0
R28	1	AB	RC07GF103F	6-172100-0

SWITCH ASSEMBLY
750-538-02, -6 configuration

CR1-4	4	FA	1N4148	1-194148-0
Q1-4	4	TS	U1897	1-241897-0
CR	1		XA2B68692F	1-436861-0
C7	1		XAB6312F	1-436311-0
C2	1		XA2B94562F	1-439451-0
C5	1		XA2B36442F	1-433641-0
C3	1		XA2B2064F	1-442061-0
C8	1		XA2B189382F	1-441891-0
C1	1		XA2B283642F	1-442831-0
CL	1		XA2B109362F	1-441091-0
S1	1			
S2	1			
U1	1		LF356N	1-100356-0
DS1	1	HP	5082-4655	4-120014-0
R52-54,56	4	AB	RC076F106	6-175100-0
R57	1	AB	RC07GF104	6-173100-0
R55	1	BO	3006P-1-503	6-452500-0
C9,10	2	SR	HY550	1-431004-0
R1-11,58	1			750-034-02
C11,12	2	AR	DM5100J	1-400103-0
C13	1	AR	DM5101J	1-401003-0
R12-15	4	ME	RN60C5123D	
R16-19	4	ME	RN55C2563D	1-103256-0
R20-23	4	ME	RN55C1283D	1-103128-0
R24-27	4	ME	RN55C6402D	
R28-31	4	ME	RN55C3202D	
R32-35	4	ME	RN55C1602D	
R36-39	4	ME	RN55C8001-D	
R40-43	4	ME	RN55C4001-D	
R44-47	4	ME	RN55C2001-D	
R48-51	4	ME	RN55C1001D	

FINAL ASSEMBLY 750-539

Latch, panel	1	SC	27-10-301-20	3-820005-0
Knob lock	1	RA	KL701	3-905044-0
Knob, 1/8"	1	RO	RB-67-0-M-L-9	4-100008-0
Knob, 1/4"	1	RO	RB67-1-M	4-100012-0
Panel, rear	1	EC		750-262-11
Panel, front	1	EC		750-264-01
Block, stop	1	EC		750-266-01
Cover, side	1	EC		750-267-11

Shield, guard	1	EC	750-268-11
Cover, front-6	1	EC	750-270-21
Cover, front-5	1	EC	750-270-31
Nut, insulated	1	EC	750-272-01
Handle	1	EC	750-273-11

ACCEPTANCE TEST PROCEDURE
BOEING PART NUMBER 63-11956
ECTRON MODEL 750EM-M557
FINAL 11/15/78

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ATP No. 2360, FINAL 11/15/78

ACCEPTANCE TEST PROCEDURE

May 5, 1978

BOEING PART NUMBER 63-11956
ECTRON MODEL 750EM-M557
General Purpose, Wide Band, Floating D.C. Differential Amplifier

1.0 GENERAL

The following describes the methods used and equipment required to validate the specifications on the 750EM-M557 amplifier as required in Boeing Specification 63-11956. The Gain/Filter assembly is type -5 and the amplifier configuration is -1.

The operating temperature range of the amplifier is 0-50 degrees C (3.1.3.1). Temperature tests have been extended from 0 to -10 degrees C to avoid possible internal condensation in the amplifier which might cause erratic results. The permissible variations in this procedure reflect the extended range.

The numbers in parentheses in this procedure are the same as the corresponding paragraph in the Specification.

Certain tests in this procedure will require test fixtures to be made as shown in the drawings at the end of this procedure. All grounds should be returned to one point as shown. Use care to shield the signal input leads right up to the input connector to avoid noise pick up and common mode rejection degradation. Tests marked with an asterisk [*] are to be performed on a sample basis.

2.0 EQUIPMENT REQUIRED

NOTE:
All equipment used to verify specification compliance must be at least three times more accurate than the measurements used to verify the specification and must be traceable to NBS.

Precision Divider (R1, Fig. 1) ESI RV622 or equivalent.

Function Generator, Wavetek 180 or equivalent.

Oscilloscope, differential, 1mV sensitivity. Tektronix 5110 main frame with 5B10N time base and 5A22N differential amplifier or equivalent. Ensure that the 5A22N has been adjusted for maximum low and high frequency common mode rejection according to the manufacturers specifications as differential measurements are used in the procedure.

Digital Multimeter/Counter, 100uV resolution. California Instruments 8420 or equivalent.

Digital Multimeter, 10uV resolution. Fluke 8040A or equivalent.

Frequency Synthesizer, Wavetek 171 or equivalent.

Variable Transformer, 1 amp. capability. GE 9T92A1 or equivalent.

Environmental Chamber (-10 to +50 degrees C)
Adequate size for amplifier.

Peak Detector, ECTRON X201 or equivalent.

Phase Meter Wavetek 740 or equivalent.

Mercury Relay Clare HG501 or equivalent.

Volt Ohmmeter, HP Model 427A or equivalent.

Null Meter, Kintel 204A or equivalent.

Power Supply 10V dc @ 0.1 amp. PS1.

Power Supply 0 - 24V dc @ 0.1 amp. PS2.

Power Supply 20V dc @ 0.1 amp., PS 3. Used for dc common mode tests (3.2.13).

Pulse Generator, Cimron 3201 or equivalent.

Sine Wave Generator 100 MHz. Tektronix SG503 Leveled Sine Wave Generator, or equivalent.

Sine Wave Oscillator H.P. 202C or equivalent.

Ectron Model 1100CF Thermocouple Simulator/Calibrator

Tektronix 545A oscilloscope with 1A1 plug in.

Miscellaneous resistors, switches, and components.

3.0 TESTS PERFORMED

3.1 Plus and minus 20 volts input overload (Fig. 15) (3.2.14)

3.1.1 Adjust PS3 to 20 volts.

3.1.2 Connect the amplifier to be tested as shown in Figure 15.

3.1.3 Position S1 to A.

3.1.4 Adjust the gain switch on the amplifier from 1 to 1000.

3.1.5 Position S1 to B.

3.1.6 Adjust the gain switch on the amplifier from 1000 to 1.

This completes the test. The overvoltage condition should not affect the specification validations which follow.

3.2 Gain Temperature Coefficient (Figure 1) (3.2.6)

3.2.1 Connect the amplifier to be tested as shown in Figure 1.

3.2.2 Set the amplifier to a gain of 1000.

3.2.3 Place the amplifier in the environmental chamber; set the chamber to 25 degrees C.

3.2.4 Set the precision divider to 001000.

3.2.5 Switch S1 from B to A and record the shift in mV as observed on the oscilloscope after temperature stabilization.

3.2.6 Set the environmental chamber to -10 degrees C.

3.2.7 Repeat step 3.2.5.

3.2.8 Set the environmental chamber to +50 degrees C.

3.2.9 Repeat step 3.2.5.

The gain temperature coefficient is determined as follows:

$$\%/\text{degree C} = \frac{(\text{Reading in 3.2.7} - \text{Reading in 3.2.5})}{(35 \times 100)} \quad \text{and}$$

$$\frac{(\text{Reading in 3.2.9} - \text{Reading in 3.2.5})}{(25 \times 100)}$$

For Example:

$$\%/\text{degree C} = \frac{(8 - 4)}{(35 \times 100)} = \frac{4}{3500} = .0011\%/\text{degree C}$$

3.3 Gain Accuracy (Figure 1) (3.2.5)

3.3.1 Connect the amplifier to be tested as shown in Figure 1. The switches remain as shown.

3.3.2 Set the gain of the amplifier to 1 and the vernier switch to fixed.

3.3.3 Adjust the trace to the center line of the graticule on the oscilloscope using the front panel RTO zero potentiometer of the amplifier.

3.3.4 Set the gain of the amplifier to 1000 and the vernier switch to fixed.

3.3.5 Adjust the trace to the center line of the graticule using the front panel RTI zero potentiometer of the amplifier.

3.3.6 Adjust the precision divider R1 to 001000.

3.3.7 When switching S1 between A and B the trace on the oscilloscope must not change more than $\pm$10mV for a gain accuracy of $\pm$0.1%.

The other gain steps are validated in the same manner. Adjust the precision divider to the reciprocal of the gain selected.

3.3.8 Record the results as this test will be repeated at the end of the A.T.P. for comparison.

3.4 Bandwidth (Fig. 4) (3.2.1)

3.4.1 Connect the amplifier to be tested as shown in Figure 4.

3.4.2 Adjust the amplifier to a gain of 1, and the filter to a wideband position.

3.4.3 Adjust the oscilloscope to 2 ms/cm line sweep and 5V/cm vertical gain, A only.

3.4.4 Position S1 to x1.

3.4.5 Adjust the function generator to 100 Hz sine wave with sufficient output to provide 4 cm vertical deflection on the oscilloscope.

3.4.6 Increase the frequency of the function generator until the amplitude is 2.83 cm (-3dB).

Note and record the frequency which must be more than 40KHz.

3.4.7 Repeat the previous steps with the amplifier at a gain of 1000. Repeat the previous steps using the filtered output in the wideband position.

3.5 Filter Response (3.2.1)

3.5.1 Filter response for filters above 100Hz. (Figure 16.)

3.5.1.2 Connect the equipment as shown in Figure 16.

3.5.1.3 Set the amplifier gain to 2.

3.5.1.4 Set the amplifier filter switch to 10KHz.

3.5.1.5 Set switch S1 to A.

3.5.1.6 Set the frequency synthesizer to a 1 KHz (.1 Fco) sine wave and adjust the amplitude for a 1.0000 V rms reading on the DMM/C. (The oscilloscope is used to monitor the waveform.)

3.5.1.7 Set the frequency to 5 KHz (.5 Fco).

3.5.1.8 Record the reading on the DMM/C.

3.5.1.9 Set the frequency to 10 KHz (Fco).

3.5.1.10 Record the reading on the DMM/C.

3.5.1.11 Set the frequency to 30 KHz (3 Fco).

3.5.1.12 Record the reading on the DMM/C.

3.5.1.13 Refer to Table I below and repeat the above procedure substituting the appropriate frequencies.

3.5.1.14 Set switch S1 to B.

3.5.1.15 Set the amplifier gain to 1000.

3.5.1.16 Repeat steps 3.5.1.4 through 3.5.1.13.

TOLERANCES:
.1Fco = reference (1.000V rms).
.5Fco = V $\pm$1.0% (10mV) amplifier to amplifier
Fco = V $\pm$1.5% (15mV) amplifier to amplifier
3Fco = <12% (120mV) of reference.

V_1 and V_2 will be determined empirically.

FILTER (Hz)	.1 Fco (Reference)	.5Fco	Fco	3Fco
10K	1K	5K	10K	30K
3K	300	1.5K	3K	9K
1K	100	.5K	1K	3K
300	30	150	300	900

TABLE I

3.5.2 Filter response for filters of 100Hz and below (figure 6).

3.5.2.1 Connect the equipment as shown in figure 6.

3.5.2.2 Set switch S1 to A.

3.5.2.3 Set the amplifier gain to 2.

3.5.2.4 Set the amplifier filter switch to 100Hz.

3.5.2.5 Set the frequency synthesizer to 10Hz (.1 Fco) sine wave and adjust the amplitude for a 1.0000 V DC reading on the DMM/C.

3.5.2.6 Set the frequency to 50Hz (.5 Fco).

3.5.2.7 Record the reading on the DMM/C.

3.5.2.8 Set the frequency to 100Hz (Fco).

3.5.2.9 Record the reading on the DMM/C.

3.5.2.10 Set the frequency to 300Hz (3 Fco).

3.5.2.11 Record the reading on the DMM/C.

3.5.2.12 Refer to Tabel II below and repeat the above procedure substituting the appropriate frequencies.

3.5.2.13 Set switch S1 to B.

3.5.2.14 Set the amplifier gain to 1000 and repeat steps 3.5.2.4 through 3.5.2.11.

TOLERANCES: .1Fco = reference (1.000V rms).
.5Fco = V ±1.0% (10mV) amplifier to amplifier
Fco = V ±1.5% (15mV) amplifier to amplifier
3Fco = <12% (120mV) of reference.

V_1 and V_2 will be determined empirically.

Filter (Hz)	.1Fco (reference)	.5Fco	Fco	3Fco
100	10	50	100	300
30	3	15	30	90
10	1	5	10	30
3	.3	1.5	3	9
1	.1	.5	1	3

TABLE II

3.6 Adjustable Gain Control (Figure 1) (3.2.3)

3.6.1 Set amp gain to 100.

3.6.2 Adjust the front panel gain potentiometer fully clockwise.

3.6.3 Position the front panel gain vernier switch to VARiable.

3.6.4 Adjust the divider until minimum scope shift is observed when switching S1 between A and B.

3.6.5 The divider setting should be 003636 or less.

3.6.6 Repeat using CCW setting of the vernier control. The divider setting must be 010000 or greater.

3.7 Zero Temperature Coefficient (Figure 1) (3.2.18)

3.7.1 Adjust the amplifier to a gain of 1000 with zero controls adjusted as in steps 3.3.2 through 3.3.5.

3.7.2 After one hour stabilization, read and record data on digital multimeter.

3.7.3 Place the amplifier to be tested in an environmental chamber programmed to -10 degrees C.

3.7.4 Record the reading on the digital multimeter (1 volt FS) after temperature stabilization. (2 hours max.)

3.7.5 Increase the temperature of the environmental chamber to 50 degrees C.

3.7.6 Record the reading on the digital multimeter after temperature stabilization. (2 hours max.)

The difference in the readings at steps 2 and 6 must be <0.4 uV x 1000 x 25 + 100uV x 25 = $\pm$12.5 mV. The difference in readings at steps 2 and 4, must be <0.4uV x 1000 x 35 + 100uV x 35 = $\pm$ 17.5 mV.

3.7.7 Reduce the gain of the amplifier to 1.

3.7.8 Repeat steps 3.7.3 through 3.7.6.

The difference between the readings in steps 3.7.4 and 3.7.6 must be less than $\pm$ 6 mV.

3.8 Calibration control relay (Figure 2) (3.2.4)

3.8.1 Connect the amplifier to be tested as shown in Figure 2.

3.8.2 Adjust the amplifier to a gain of 20.

3.8.3 Set the Fluke 8040A to 10uV DC resolution.

3.8.4 Adjust the precision divider to 0-2-5-0-0-0.

3.8.5 Adjust the decade switches on the Model 1100CF to +5000.0 mV.

3.8.6 Switch S1 to A.

3.8.7 Note the reading on the Fluke 8040A to the nearest 10uV's.

3.8.8 Switch S2 to A.

3.8.9 Note the reading on the Fluke 8040A to the nearest 10uV's.

The difference between the readings noted in steps 3.8.7 and 3.8.9 must be <$\pm$150uV.

3.9 *Calibration Temperature Coefficient (Figure 2)

3.9.1 Place the amplifier to be tested in an environmental chamber programmed to -10 degrees C.

3.9.2 Repeat Section 3.8, and record the difference between readings in sections 3.8.7 and 3.8.9.

3.9.3 Increase the temperature of the environmental chamber to 50 degrees C.

3.9.4 Repeat Section 3.8, and record the difference between readings in sections 3.8.7 and 3.8.9.

The permissible difference between readings in sections 3.9.2 and 3.9.4 is 600uV.

3.10 Linearity (Figure 7) (3.2.7)

3.10.1 Adjust the amplifier to a gain of 1000 (3.2.5).

3.10.2 Connect the amplifier as shown in figure 7.

3.10.3 Adjust the function generator for an output of 20V p-p 1 Hz triangular wave.

3.10.4 Adjust the precision divider R1 to 001000.

3.10.5 Adjust the oscilloscope to 1 mV/cm and the horizontal input vernier to present a ±5 cm trace.

3.10.6 Trim the precision divider R1 and/or the gain vernier to present the best possible horizontal trace.

The maximum permissible deviation from a straight line is plus or minus 1mV.

This test also verifies the output voltage specification of ± 10V.

3.10.7 Repeat steps 3.10.1 through 3.10.6 using the filtered output.

3.10.8 *Set the precision divider to 999999, amplifier gain to 1000. Verify that no foldover occurs.

3.11 Capacitive Loading (Figure 4) (3.2.10)

3.11.1 Set the amplifier to a gain of 1000.

3.11.2 Adjust the function generator for a 100Hz 20V p-p square wave.

3.11.3 Add capacitive loads from 100pf to 0.22mf with at least 3 steps per decade while observing the square wave on the oscilloscope.

3.11.4 Repeat 3.11.1 through 3.11.3 at the filtered output.

No instability shall occur.

3.12 Input Impedance (Figure 1) (3.2.8)

3.12.1 Connect the amplifier to be tested as shown in Figure 1.

3.12.2 Set the amplifier to a gain of 1000.

3.12.3 Note the reading on the DVM.

3.12.4 Switch S1 to A and note the reading on the DVM.

3.12.5 Record the difference in mV between 3.12.3 and 3.12.4 as gain error 1.

3.12.6 Switch S1 to B.

3.12.7 Open S2.

3.12.8 Note the reading on the DVM.

3.12.9 Switch S1 to A and note the reading on the DVM.

3.12.10 Record the difference in mV between 3.12.7 and 3.12.8 as gain error 2.

3.12.11 Calculate input impedance as follows:

$$Z \text{ in} = \frac{100 \text{ M}}{\text{Gain error 1} - \text{Gain error 2}}$$

e.g., $\frac{100 \text{ M}}{9 - 5} = \frac{100\text{M}}{4} = 25 \text{ M ohms}$

3.12.12 Set S4 to A, the Ectron 1100CF to -9999.9 mV, and repeat steps 3.12.3 through 3.12.10 substituting S3 for S2 in step 3.12.6.

3.12.13* Repeat the procedure at a gain of 1.

The input impedance must be greater than 10M ohms.

3.13 Input and Calibration Isolation (Figure 14) (3.2.8)

3.13.1 Connect the amplifier to be tested as shown in Figure 14. The amplifier need not be energized for this test. The switches remain as shown.

The reading on the HP427A must be more than 100 M ohms.

3.13.2 Position S1 to B and S2 to B.

The reading on the HP427A must be more than 100 M ohms.

3.14 * Input Capacitance (Figure 8) (3.2.8)

Note: The following test is done with the amplifier in an enclosure.

3.14.1 Adjust the gain of the amplifier to 1000.

3.14.2 Install the amplifier in an enclosure and connect as shown in Figure 8. Ensure that the corresponding input and output connectors are used.

3.14.3 Adjust the function generator to 100 Hz sine wave, and sufficient amplitude to display 5.000V ac on the multimeter.

3.14.4 Increase the frequency of the function generator until the display reads 3.540 volts(-3dB).

The frequency must be over 4.905KHz, which indicates an input capacitance less than 500 pf.

3.14.5 Position S1 to B and repeat steps 3.14.3 and 3.14.4.

3.15 Pumpout Current (Figure 1) (-10 to +50 degrees C) (3.2.8)

3.15.1 Connect the amplifier to be tested as shown in Figure 1. The switches remain as shown.

3.15.2 Adjust the amplifier to a gain of 100.

3.15.3 Adjust the precision divider to 000000.

3.15.4 Record the reading on the digital multimeter.

3.15.5 Open S2.

3.15.6 Record the reading on the digital multimeter.

3.15.7 Close S2 and open S3.

3.15.8 Record the reading on the digital multimeter.

The difference between the readings in 3.15.6 and 3.15.4 also 3.15.8 and 3.15.4 must be less than 5 mV for a pumpout current less than 5 nA.

The previous tests shall be repeated at -10 degrees and 50 degrees C to ensure the pumpout current does not exceed 5 nA. Close S2 and S3 upon completion of test.

3.16 Output Impedance (Figure 4) (3.2.9)
Note: Use the test connections for bandwidth as shown in Figure 4.

3.16.1 Adjust the amplifier to a gain of 1.

3.16.2 Set the function generator to 40KHz, sine wave output.

3.16.3 Adjust the output level of the function generator to display 7.000 volts ac on the digital multimeter.

3.16.4 Connect a 125 ohm 1 watt resistor right at pins 29 and 30 of the output connector to avoid IR losses.

3.16.5 Record the reading on the digital multimeter.

3.16.6 Repeat using the filter output in the wideband position.

3.16.7 *Repeat sweeping the function generator from 1KHz to 40KHz.

The reading on the digital multimeter recorded in step 3.16.5 must be less than 11mV (6.989V) from the reading recorded in step 3.16.3 indicating Zo <0.2 ohms.

3.17 Output Current (Figure 1) (3.2.12)

Repeat the linearity test (3.10, [3.2.7]) with a 125 ohm load. The maximum permissible deviation is plus or minus 100mV.

3.17.1 Connect the amplifier to be tested as shown in Figure 1.

3.17.2 Adjust the amplifier to a gain of 100.

3.17.3 Adjust the precision divider to 010000.

3.17.4 Position S1 to A.

3.17.5 Connect a 50 ohm 2 watt resistor across the output terminals of the amplifier.

The display on the digital multimeter must be between 4.0 and 5.0 V. Repeat test at filtered output and negative output voltages.

Repeat the above tests at -10 and +50 degrees C.

3.18 Common Mode Rejection (Figure 3) (3.2.13.1)

NOTE: Check each input with source R and take data on worst input.

3.18.1 dc, 1K ohm source R

3.18.1.1 Adjust the amplifier to a gain of 1000 (3.2.5) and wideband.

3.18.1.2 Install 1000 ohm resistors for Rx in Figure 3.

3.18.1.3 Connect the amplifier to be tested as shown in Figure 3.

3.18.1.4 Position S3 to B.

3.18.1.5 Center the trace on the oscilloscope.

3.18.1.6 Connect the 20 volt power supply PS3 to give +20 volts common mode voltage.

3.18.1.7 Position S3 to A.

3.18.1.8 Record the dc shift on the oscilloscope.

The dc shift must be less than 20 mV for a rejection greater than 60dB + 60dB (A = 1000).

Repeat 3.18.1.6 thru 3.18.1.8 with PS3 connected for -20V.

3.18.1.9 Position S3 to B.

3.18.2 100 Hz, 1K ohm source R (Figure 3)

3.18.2.1 Substitute the sine wave oscillator for the ± 20 volt power supply PS3 in Figure 3.

3.18.2.2 Position S3 to A.

3.18.2.3 Adjust the sine wave oscillator to 40V p-p sweep from 5Hz to 100Hz.

3.18.2.4 Record the maximum residual trace on the oscilloscope.

The residual trace must be less than 40 mV p-p for a rejection greater than 120dB.

3.18.3 1KHz, 1K ohm source R

3.18.3.1 Sweep the sine wave oscillator from 100Hz to 1KHz.

The residual trace on the oscilloscope must be less than those shown on Table 1.

3.18.4 20 KHz, 1K ohm source R

3.18.4.1 Sweep the sine wave oscillator from 1KHz to 20KHz, reducing the amplitude proportionally with frequencies to 2V p-p at 20KHz.

The residual trace on the oscilloscope must be less than those of Table 1.

3.18.5 100KHz, 1K ohm source R

3.18.5.1 Sweep the frequency of the function generator to 100KHz. The amplitude and function remain at 2V p-p sine wave.

The residual trace must be less than those of Table 1.

3.18.6 Sweep the frequency of the function generator to 1 MHz. The amplitude remains at 2V p-p.

The deviation on the oscilloscope must be less than ± 1 volt for all frequencies.

3.18.7 Remove the function generator (Figure 3) and connect the Tektronix SG503. Note that 50 ohm cable must be used and that the cable must be terminated into 50 ohms.

3.18.8 Adjust the output of the Tektronix SG503 to 2V p-p at 100KHz.

3.18.9 Position S3 to A.

3.18.10 Slowly increase the frequency to 100MHz.

The deviation on the oscilloscope must be less than ±1 volt for all frequencies.

3.18.11 The preceding tests are repeated with S1 closed and S2 open.

3.19 DC Offset (Figure 3) (3.2.13.2)

3.19.1 Connect the amplifier (A=1000) as shown in figure 3. Be sure to include the 1Hz filter as shown.

3.19.2 Close S1, S2, and position S3 to B.

3.19.3 Adjust the scope for 0.5 mV/cm and 2 ms line sync.

3.19.4 Open S1.

3.19.5 Center the trace on the graticule using the RTI Zero Pot.

3.19.6 Connect the sine wave oscillator.

3.19.7 Adjust the sine wave oscillator to 40V p-p and sweep from 10Hz to 100Hz.

The deviation on the oscilocope must be less than ±4 cm for ±2mV offset.

3.19.8 Repeat step 19.7 using 20V p-p and sweep from 100Hz to 10KHz.

3.19.9 Repeat step 19.7 using 2V p-p and sweep from 10KHz to 100KHz.

3.20.0 Step Response (Figure 9) (3.2.14)

3.20.1 Full Scale Recovery

3.20.1.1 Connect the equipment as shown in Figure 9.

3.20.1.2 Set the amplifier to a gain of 10.

3.20.1.3 Position S1 and S2 to +.

3.20.1.4 Position S3 open, S4 to 2, S5 to A.

3.20.1.5 Adjust the function generator and pulse generator to obtain a 20ms pulse with a repetition rate of 1Hz.

3.20.1.6 Adjust PS3 to obtain a ten-volt square wave as seen on the oscilloscope. Make sure that the scope is being triggered by the pulse generator and that the sweep starts on a vertical graticule line.

3.20.1.7 Position S5 to B and adjust the oscilloscope vertical sensitivity to 1mv/cm. Observe recovery time.

3.20.1.8 Set the amplifier gain to 1000. Set S4 to 3, S5 to A.

3.20.1.9 Repeat steps 3.20.1.6 and 3.20.1.7.

3.20.1.10 Set S1 and S2 to -, and the pulse generator for negative pulses.

3.20.1.11 Repeat steps 3.20.1.4 through 3.20.1.9.

The amplifier output shall settle within $\pm$ 1mv in less than 200us, and shall remain there for an observed time of one second or more.

3.20.2 500% Overload Recovery

3.20.2.1 Connect the amplifier to be tested as shown in Figure 9.

3.20.2.2 Set the amplifier gain to 1.

3.20.2.3 Set S1 and S2 to +.

3.20.2.4 Position S3 closed, S4 to 2, and S5 to A.

3.20.2.5 Adjust the function generator to obtain a 50 ms pulse with a repetition rate of 1Hz.

3.20.2.6 Adjust PS3 to obtain a 5 volt square wave as seen on the oscilloscope.

3.20.2.7 Set the amplifier gain to 10, set the scope vertical sensitivity to 5mv/cm. Record the recovery time.

3.20.2.8 Set S4 to 3, set the amplifier gain to 100.

3.20.2.9 Repeat 3.20.2.6.

3.20.2.10 Adjust the amplifier gain to 1000. Record the recovery time.

3.20.2.11 Set S1 and S2 to -, and the pulse generator for negative pulses.

3.20.2.12 Repeat steps 3.20.2.4 through 3.20.20.2.10.

The amplifier output shall recover within ± 5mv in less than 400us and remain there for an observed time of one second or more.

3.20.3 20-Volt Overload Recovery

3.20.3.1 Connect the amplifier to be tested as shown in Figure 9.

3.20.3.2 Set S1 and S2 to +, S3 closed, S4 to 1, S5 to B.

3.20.3.3 Momentarily connect the scope to the wiper of S4 and adjust the function generator, PS3, and the pulse generator for a pulse of 20V amplitude, 20ms width and a 1Hz repetition rate.

3.20.3.4 Reconnect the scope as shown in Figure 9.

3.20.3.5 Set the amplifier gain to 10, and the scope sensitivity to 5mv/cm. Record the recovery time.

3.20.3.6 Set the amplifier gain to 1000. Record the recovery time.

3.20.3.7 Set S1 and S2 for -, and the pulse generator for negative pulses.

3.20.3.8 Repeat steps 3.20.3.3 through 3.20.3.6.

The amplifier output shall recover within ± 5mv in less than 10ms and remain there for an observed time of one second or more.

3.21 Overload indication (Figure 10) (3.2.14.1)

3.21.1 Adjust the function generator to 20V p-p square wave at 100Hz. (Figure 10)

3.21.2 Adjust P.S.3 to 20 volts.

3.21.3 Adjust the gain of the amplifier to 1 and connect as shown in Figure 10.

3.21.4 Position S2 to A.

3.21.5 Close S1 momentarily.

3.21.6 Measure the dc voltages on TP2 and TP3 in respect to TP1.

Both voltages should read +20V.

3.21.7 Adjust PS2 to 10.0V.

3.21.8 Position S2 to B.

The overload indicator on the front panel should not be illuminated.

3.21.9 Increase the voltage of PS2 until the indicator turns on.

3.21.10 Record the voltage of PS2.

3.21.11 Reverse the polarity of the power supply.

3.21.12 Repeat steps 3.21.7 through 3.21.10

The overload indicator on the front panel should be illuminated. The dc voltage at TP2 and TP3 should be less than 0.5 volts.

3.21.13 Adjust the power supply PS 2 to zero.

The voltage at TP2 and TP3 should be 0.5 volts and 20 volts respectively.

3.21.14 Close, then open S1.

The voltage at TP2 and TP3 should be 20 volts.

3.21.15 The current into pins 21 and 23 is 3.5 mA when the internal transistors are in the "on" state and the voltage is 20 volts when the internal transistors are in the "off" state. This exceeds the specification of 2 x 1.6 mA and 15 volt pull up.

3.21.16 Connect the amplifier as shown in Figure 20.

3.21.17 Set the amplifier gain to 2.

3.21.18 *Adjust the pulse generator for a 10ms pulse in the single pulse mode. Depress the single pulse button while observing the signal at TP3 with the scope. The signal should be near zero for approximately 100ms.

3.22 Offset Adjustment (Figure 3) (3.2.15)

3.22.1 Connect the amplifier to be tested as shown in Figure 3.

3.22.2 Position S3 to B.

3.22.3 Adjust the gain of the amplifier to 1.

3.22.4 Connect a digital multimeter across the output of the amplifier.

3.22.5 Adjust the amplifier output to maximum positive and negative range using the front panel RTO zero potentiometer.

Note that the resolution of the RTO zero potentiometer is better than 500 uV and that the span is greater than ±80 mV and that at least 20 mV on either side of zero can be attained.

3.23 Noise (Wideband Output, Figure 12) (3.2.19)

3.23.1 Adjust the amplifier to a gain of 1.

3.23.2 Open S1 or S2, Figure 12.

3.23.3 Connect the 545A oscilloscope with 1A1 plug in as shown. Connect the channel 1 output output to the channel 2 input. Position the mode switch to Channel B. Adjust the gains on both channels to 0.005V/cm. The input then has a sensitivity of 0.5mV/cm.

The amplitude of the trace must be less than 1.6 cm p-p (99.7% confidence).

3.23.4 Adjust the gain of the amplifier to 1000.

3.23.5 Position the mode switch on the 1A1 to channel A and the sensitivity to 10mV/cm.

The amplitude of the trace must be less than 2.8/cm p-p (99.7 confidence).

3.24.0 Reduced bandwidth noise RTI (Figure 3) (3.2.20)

Note: The following tests are taken on the filtered output (31 high and 32 low). Use the 50KHz filter between amplifier and oscilloscope.

3.24.1 Connect the amplifier to be tested as shown in Figure 3. Be sure connections are made to the filtered output.

3.24.2 Adjust the amplifier to a gain of 1000 (3.2.5) and the filter switch to wideband.

3.24.3 Install the 50KHz filter as shown in Figure 3. The 5A22N filter must be in the 1MHz position. The noise must be less than 19mV p-p.

3.24.4 10Hz to 10KHz bandwidth

3.24.4.1 Set the amplifier filter to 10KHz. The noise must be less than 10mV p-p.

3.24.4.2 Set the amplifier filter to 1KHz. The noise must be less than 6mV p-p.

3.24.4.3 Set the amplifier filter to 100Hz. The noise must be less than 3mV p-p.

3.24.4.4 Set the amplifier filter to 10Hz. The noise must be less than 1mV p-p.

3.24.5 Reduced bandwidth noise, RTO

3.24.5.1 Adjust the amplifier to a gain of 1.

3.24.5.2 Repeat step 3.24.4.

The noise must be less than:

50KHz bandwidth	1mV p-p
10KHz bandwidth	600uV p-p
1KHz bandwidth	400uV p-p
100Hz bandwidth	300uV p-p
10Hz bandwidth	200uV p-p

3.25.0 Noise susceptibility (Figure 11) (3.2.21)

3.25.1 Status interrogation and V CAL

3.25.1.1 Connect the amplifier to be tested as shown in Figure 11.

3.25.1.2 Adjust the amplifier to a gain of 1000 (3.2.5).

3.25.1.3 Record the reading of the zero offset on the digital multimeter (1V FS) when connected to the filtered output. The digital multimeter must change less than ±500uV measured at the filtered output as the following frequencies and amplitudes are applied to the status interrogation and V CAL control lines and less than ±1.5 mV measured at the wideband output. Sweep the oscillator between the following frequencies:

Frequency	Volts p-p
10KHz - 1MHz	1.0
1-2MHz	0.5
2-3MHz	0.33
3-4MHz	0.25
4-5MHz	0.20
5-6MHz	0.17
6-7MHz	0.15
7-8MHz	0.13
8-9MHz	0.11
9-10MHz	0.10

3.25.2 Overload reset lines (Figure 11)

3.25.2.1 Connect the amplifier to be tested as shown in Figure 11.

3.25.2.2 Adjust the amplifier to a gain of 1000. (3.2.5)

3.25.2.3 Record the reading of the zero offset on the digital multimeter when connected to the filtered output. The digital multimeter must change less than ±500uV as the following frequencies are applied to the overload reset lines and less than ±1.5mV measured at the wideband output. Sweep the oscillator between the following frequencies:

Frequency	Volts p-p
10KHz to 1MHz	5.00
1 - 2	2.50
2 - 3	1.65
3 - 4	1.25
4 - 5	1.00
5 - 6	0.85
6 - 7	0.75
7 - 8	0.65
8 - 9	0.55
9 - 10	0.50

3.26 Crosstalk (Figure 13) (3.2.22)

This validation requires that three amplifiers be installed in adjacent positions in an enclosure. The outside amplifiers are driven, and the center amplifier is examined for crosstalk.

3.26.1 Select three amplifiers and adjust their gain to 1.

3.26.2 Connect a 1K ohm load resistor across the wideband outputs of two of the amplifiers.

3.26.3 Connect a 1K ohm source resistor in series with one of the inputs on the center amplifier.

3.26.4 Adjust the function generator to 20V p-p, 40KHz sine wave.

3.26.5 Adjust the center amp for gain = 1000.

3.26.6 Check for RTI noise in excess of that specified. (28 mV p-p RTO)

3.27 Slew Rate (Figure 4) (3.2.23)

3.27.1 Connect the amplifier to be tested as shown in Figure 4.

3.27.2 Adjust the gain of the amplifier to 1.

3.27.3 Position S1 (Figure 4) to x1.

3.27.4 Adjust the function generator for a 1KHz square wave output.

3.27.5 Adjust the amplitude of the function generator to display 20V p-p on the oscilloscope.

3.27.6 Measure the voltage rate of change. It must be 2.5V/us or greater.

3.28 *Short Circuit Protection (Figure 4) (3.2.24)

3.28.1 Connect the amplifier to be tested as shown in Figure 4.

3.28.2 Adjust the gain of the amplifier to 1000.

3.28.3 Set S1 to x1000 and the function generator to 20V p-p.

3.28.4 Connect a direct short across both output of the amplifier for 30 minutes.

3.28.5 Remove the direct short and determine that the amplifier operates normally.

3.29 Zero Shift with Switching (3.2.26)

3.29.1 Connect the amplifier as shown in Figure 1.

3.29.2 Adjust the precision divider to 99999(10).

3.29.3 Position S1 to B with S2 and S3 closed.

3.29.4 Set the gain of the amplifier to 1000 and adjust the trace to the center line of the graticule using the RTO zero potentiometer on the amplifier.

3.29.5 Adjust the gain of the amplifier to 1000.

3.29.6 Restore the trace to the center line of the graticule using the RTI zero potentiometer.

3.29.7 Repeat 3.29.4 through 3.29.6 until no variation occurs.

3.29.8 Switch the amplifier through all gain and filter ranges. The trace must be stable within 1mV.

3.30 Gain Accuracy (3.2.6)

Repeat 3.3 (3.2.5). Compare results with original readings. The maximum permissible deviation is ±1mV.

3.31 Output Guarding (Figure 17) (3.2.25)

3.31.1 De-energize the amplifier to be tested.

3.31.2 Connect the amplifier as shown in Figure 17.

3.31.3 Set the VOM to measure 100 M ohms.

The isolation shall be greater than 100 M ohms.

3.31.4 Switch S1 to B.

3.31.5 Energize the amplifier.

3.31.6 Set the DVM to 1 volt full scale AC.

3.31.7 The reading on the DMM shall be less than 1mv, which indicates a leakage current of less than 100nA.

3.32 Mechanical Dimensions (Figure 18) (3.1.7.2)

3.32.1 Verify the following amplifier dimensions: (See Figure 18)

A	.080 ± .040 inches.
B	.690 ± .020 inches.
C	1.560 ± .030 inches.
D	.780 ± .015 inches.
E	17.920 ± .020 inches.

3.33 Code Verification (Figure 19) (3.1.7.1,3.1.10)

3.33.1 Connect the amplifier as shown in Figure 19.

3.33.2 Verify that LED's A and C are on, and LED B is not on.

3.33.3 Switch the gain and filter switch through all positions. Verify the LED's D through G and H through L indicate the correct binary encoding for the octal code indicated in specification.

3.33.4 Operate the Vernier IN/OUT switch and verify that LED M is illuminated with the switch in the out position only.

3.34 Output Low Tests

3.34.1 De-energize the amplifier and remove it from the test adaptor.

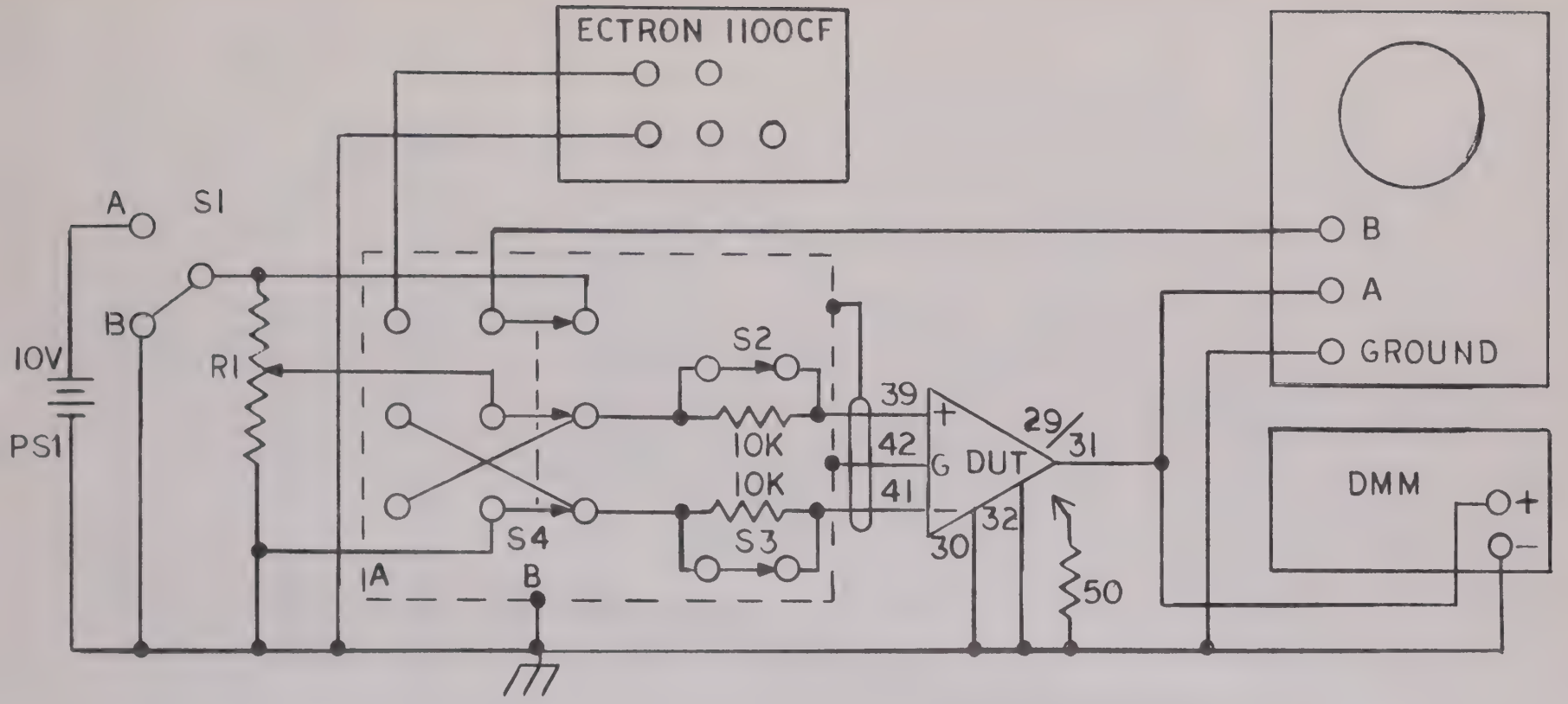
3.34.2 Verify that from the front panel to output low (pins 30 and 32) measures <1 ohm.

3.34.3 Verify that from the locking pawl to output low measures >10M ohms.

TABLE III

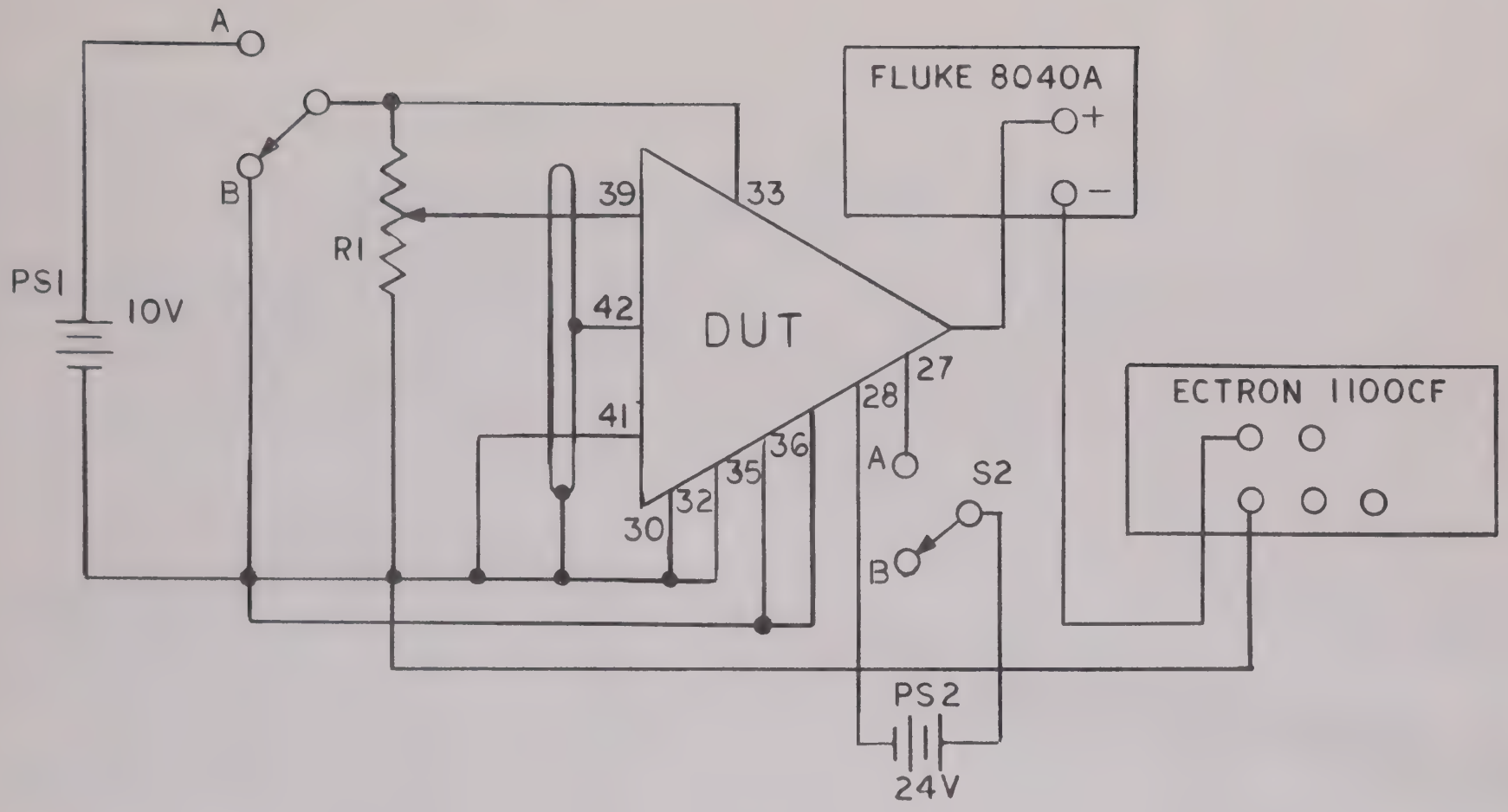
COMMON MODE REJECTION

Applied Frequency	Applied CMV P-P	Maximum Residual Voltage P-P	Equivalent Rejection Ratio
5 to 100Hz	40V	40 mv	120 dB
200Hz	40V	80 mv	114 dB
300Hz	40V	120 mv	110.5 dB
400Hz	40V	160 mv	108 dB
500Hz	40V	200 mv	106 dB
700Hz	40V	280 mv	103 dB
1 KHz	40V	400 mv	100 dB
2 KHz	20V	400 mv	94 dB
3 KHz	13.33V	400 mv	90.5 dB
4 KHz	10V	400 mv	88 dB
5 KHz	8V	400 mv	86 dB
7 KHz	5.71V	400 mv	83 dB
10KHz	4V	400 mv	80 dB
20KHz	2V	400 mv	74 dB
30KHz	2V	600 mv	70.5 dB
40KHz	2V	800 mv	68 dB
50KHz	2V	1 V	66 dB
70KHz	2V	1.4 V	63 dB
100KHz	2V	2 V	60 dB



3.2 GAIN TEMP COEFFICIENT
3.3,3.30 GAIN ACCURACY
3.6 ADJ GAIN CONTROL
3.7 ZERO TEMP COEFFICIENT
3.12 INPUT IMPEDANCE
3.15 PUMPOUT CURRENT
3.17 OUTPUT CURRENT
3.29 ZERO SHIFT WITH SWITCHING

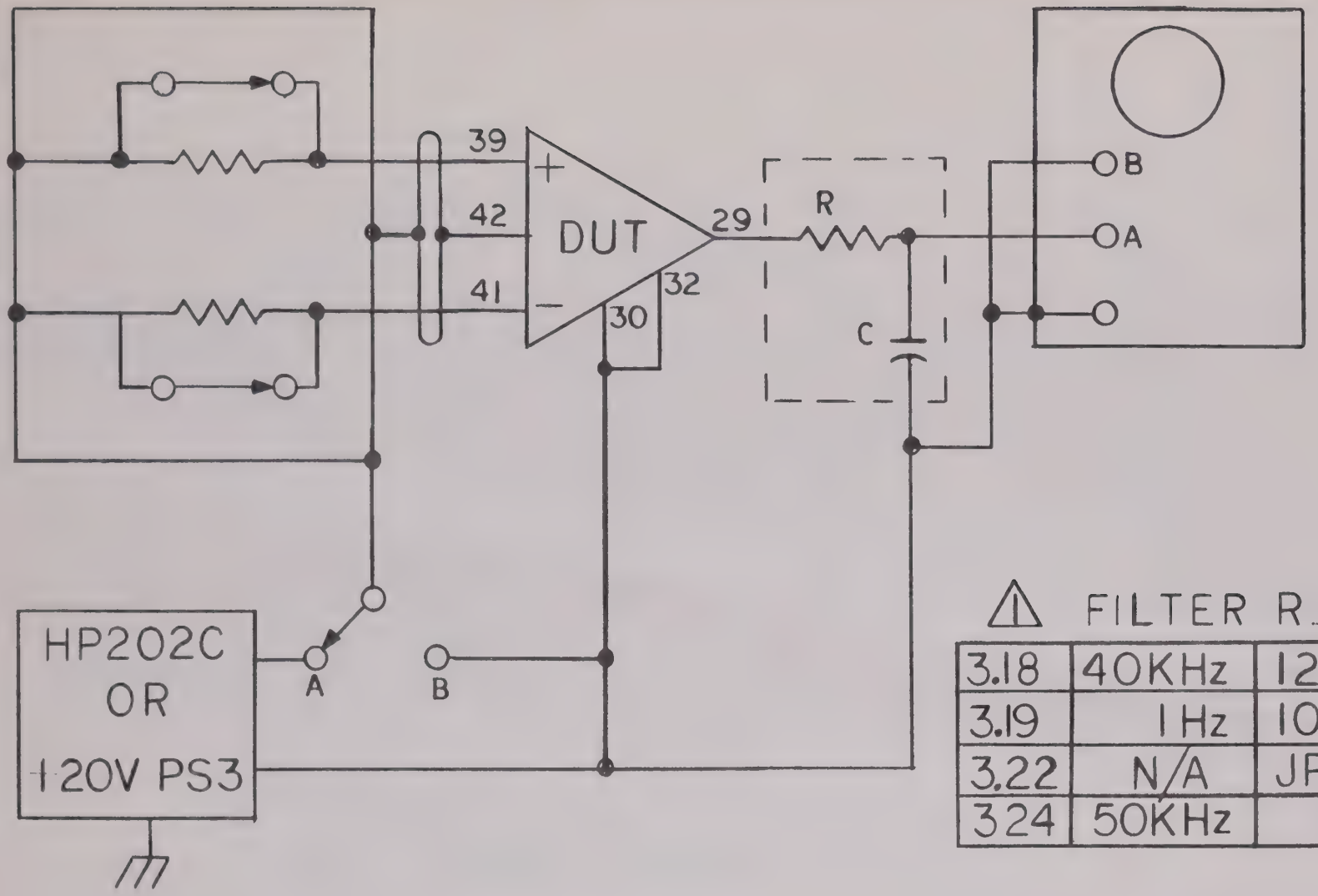
FIGURE 1



38 CALIBRATION CONTROL RELAY

39 CALIBRATION TEMPERATURE COEFFICIENT

FIGURE 2

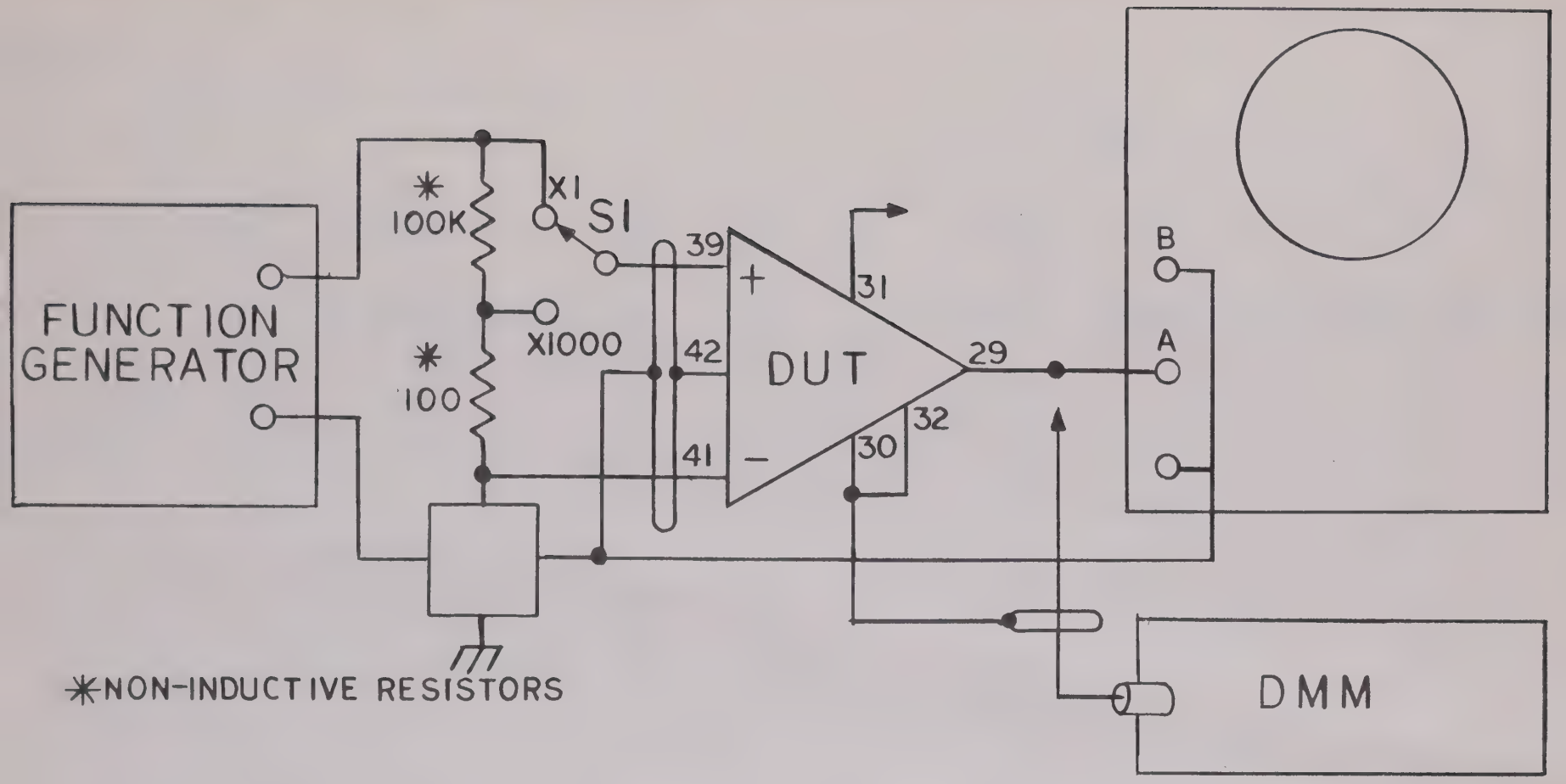


⚠	FILTER	R Ω	C uF
3.18	40KHz	12K	.0032
3.19	1Hz	10K	15
3.22	N/A	JPR	N.U.
324	50KHz	1K	.0032

TEST CONNECTIONS

3.18 COMMON MODE REJECTION
3.19 D.C. OFFSET
3.22 OFFSET ADJUST
3.24 REDUCED BANDWIDTH

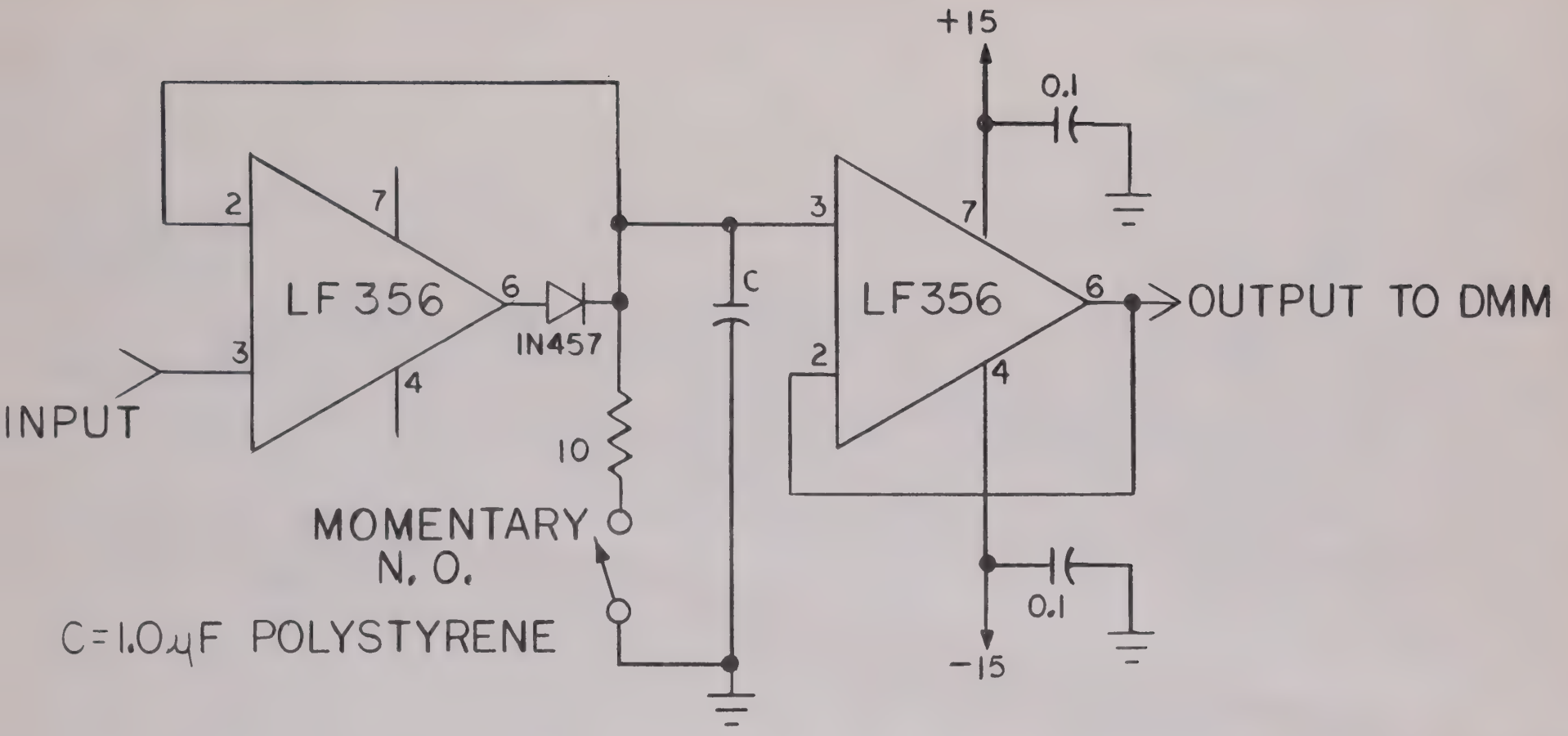
FIGURE 3



TEST CONNECTIONS

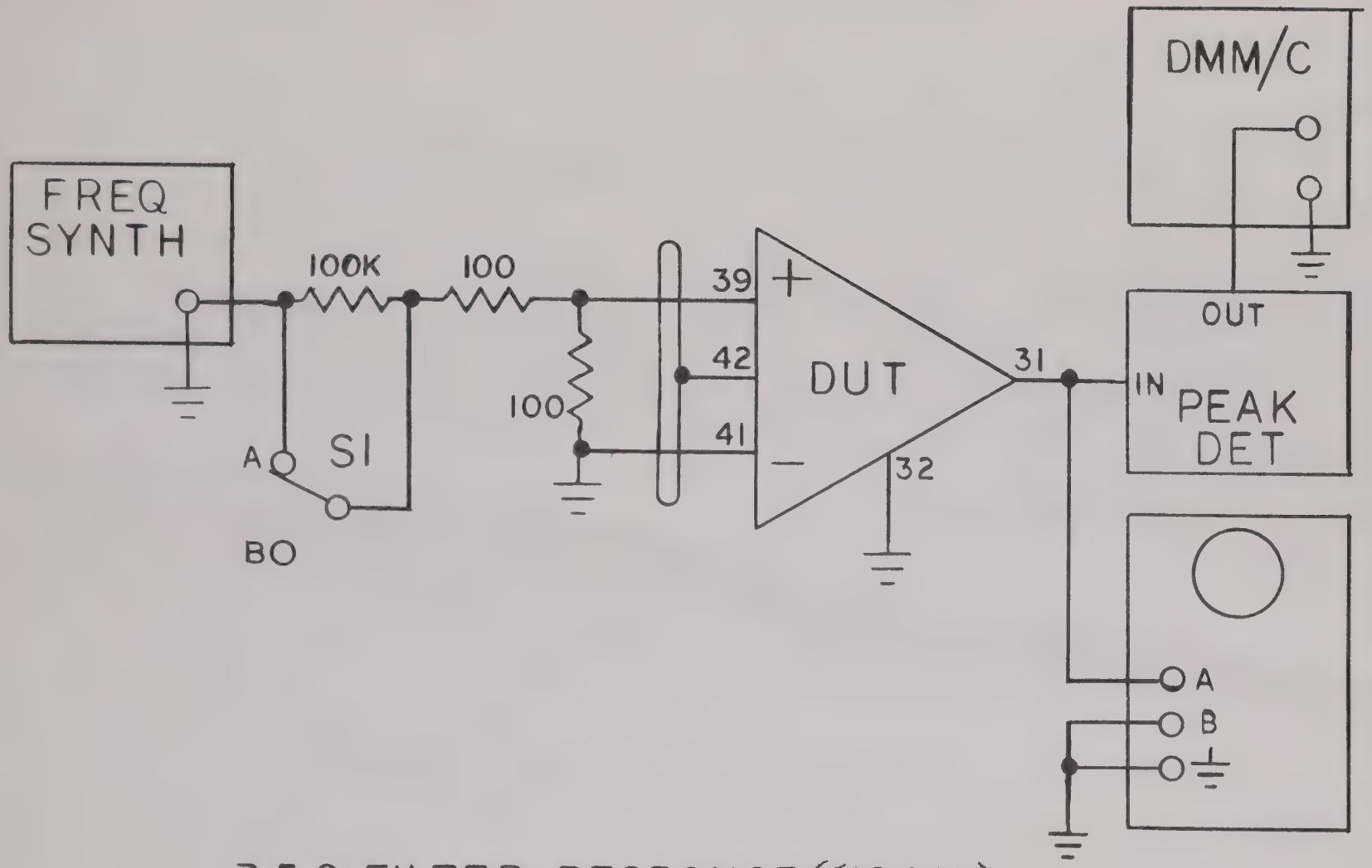
3.4 BANDWIDTH
3.16 OUTPUT IMPEDANCE
3.27 SLEW RATE
3.11 CAPACITIVE LOADING
3.28 SHORT CIRCUIT PROTECTION

FIGURE 4



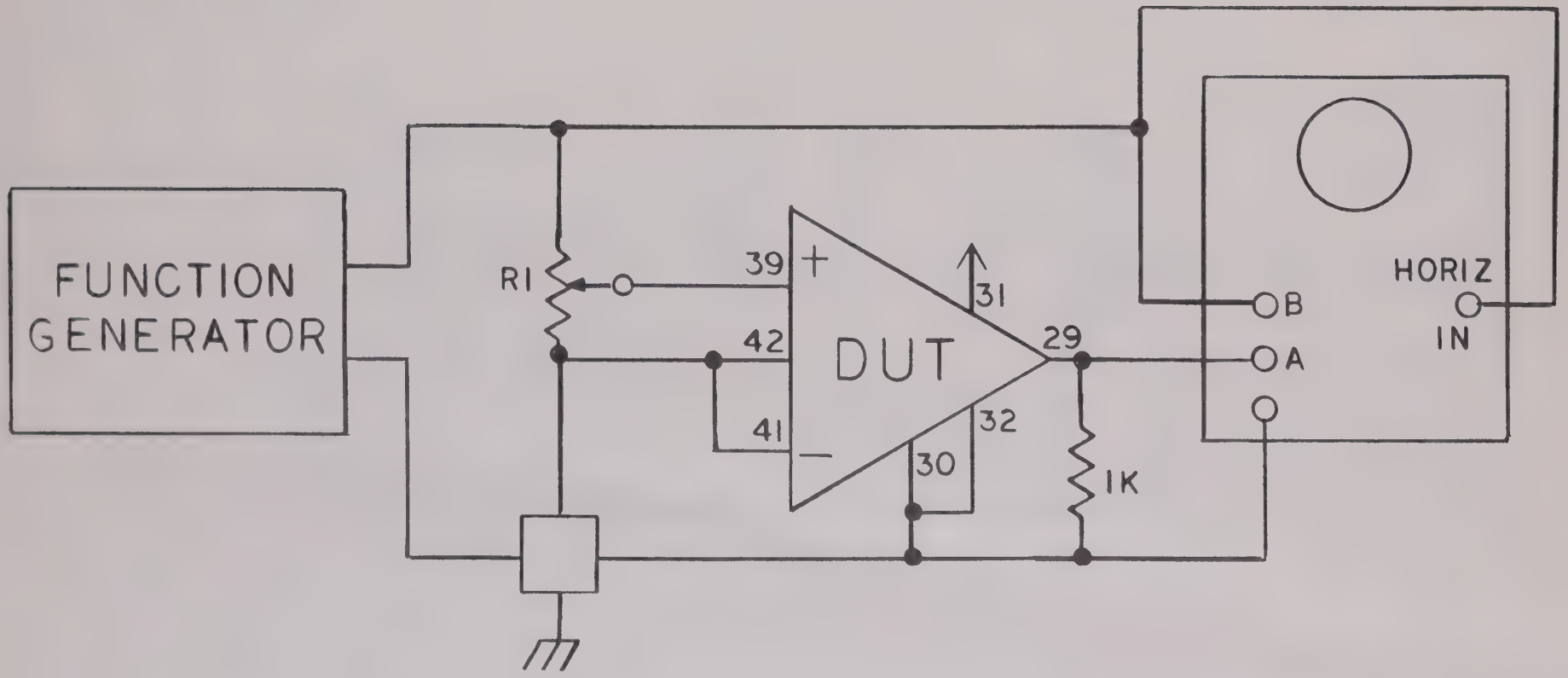
SCHEMATIC
ECTRON MODEL X201
PEAK DETECTOR
(SEE FIG 6.)

FIGURE 5



3.5.2 FILTER RESPONSE (≤100 Hz)

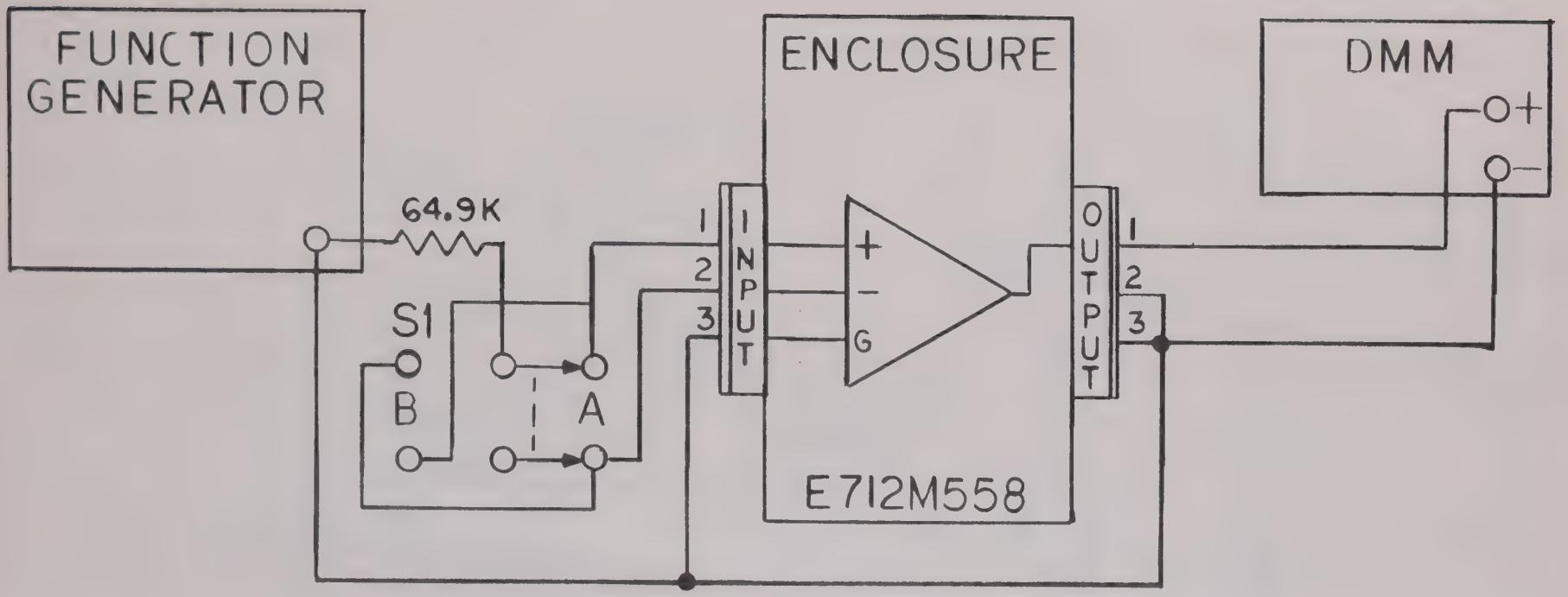
FIGURE 6



TEST CONNECTIONS

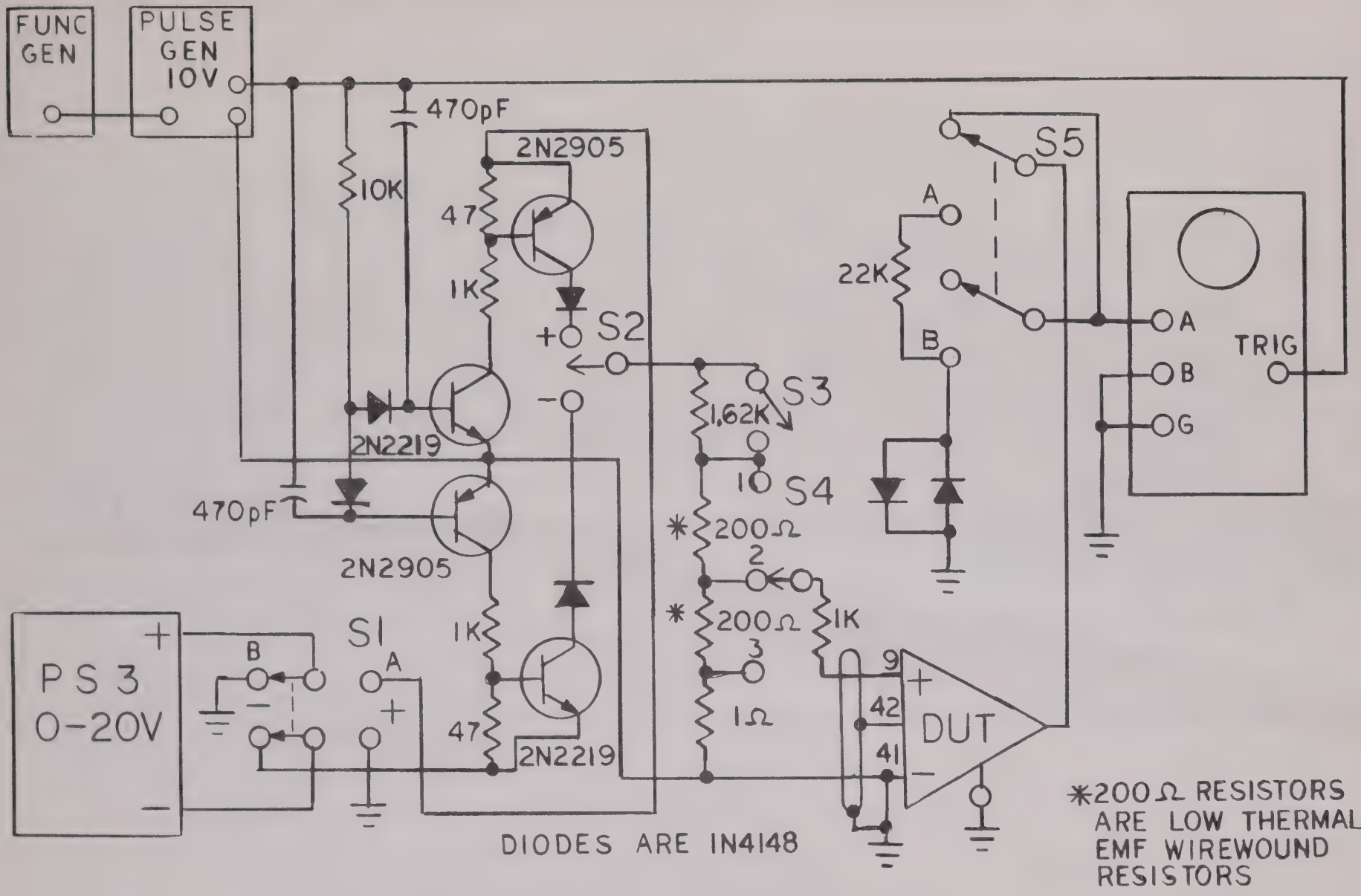
3.10 LINEARITY

FIGURE 7



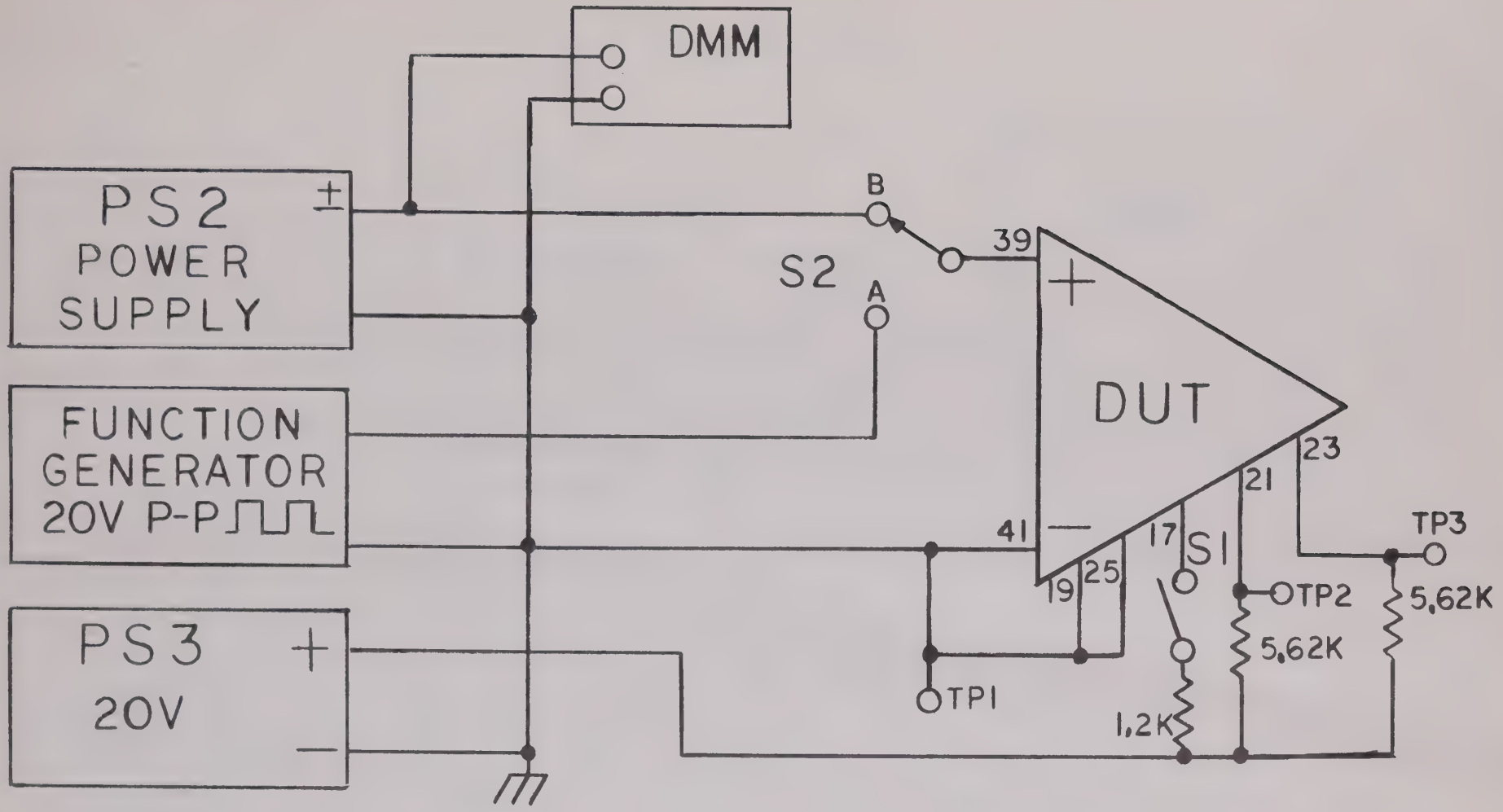
3.14 INPUT CAPACITANCE

FIGURE 8



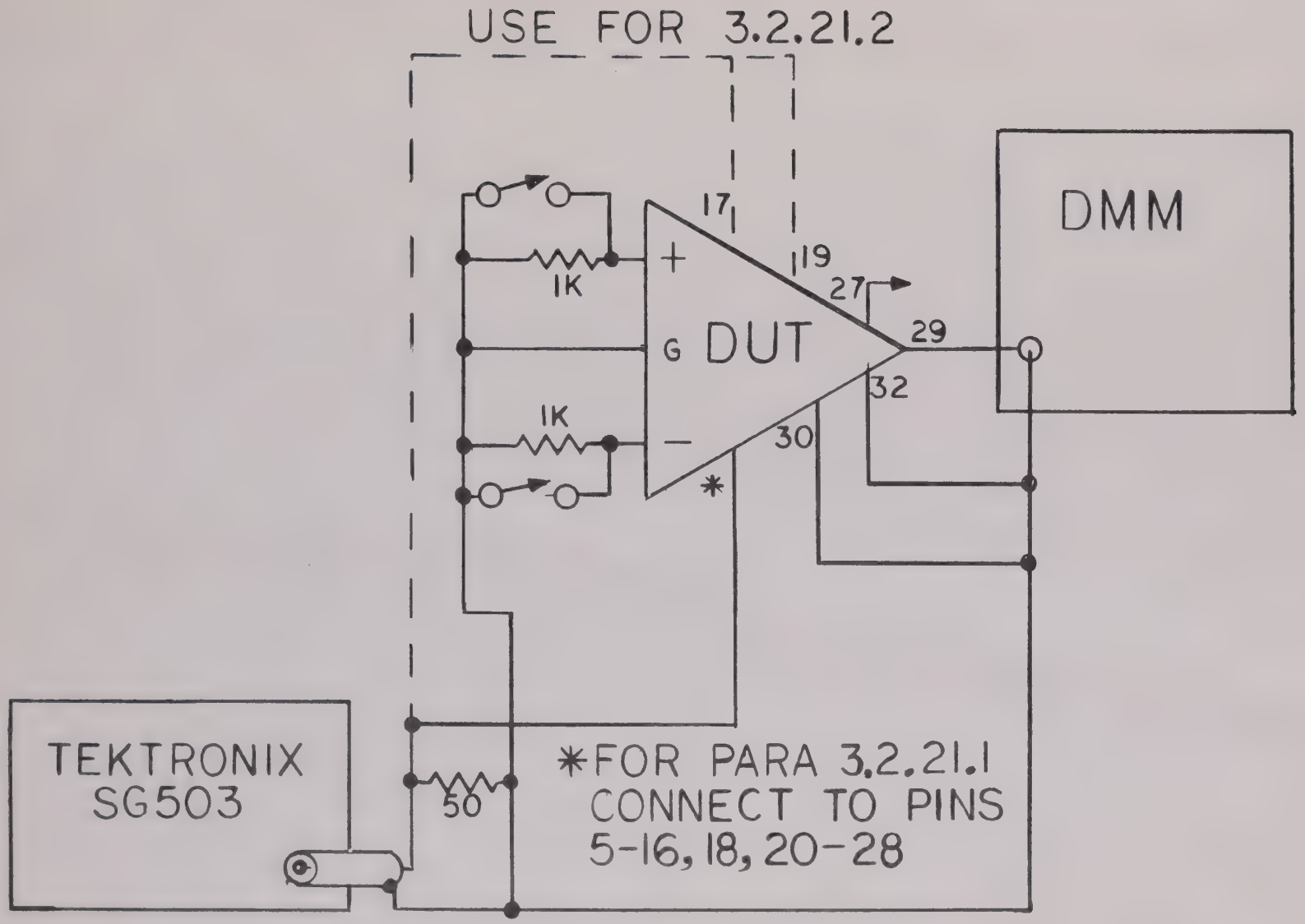
3.20 STEP RESPONSE

FIGURE 9



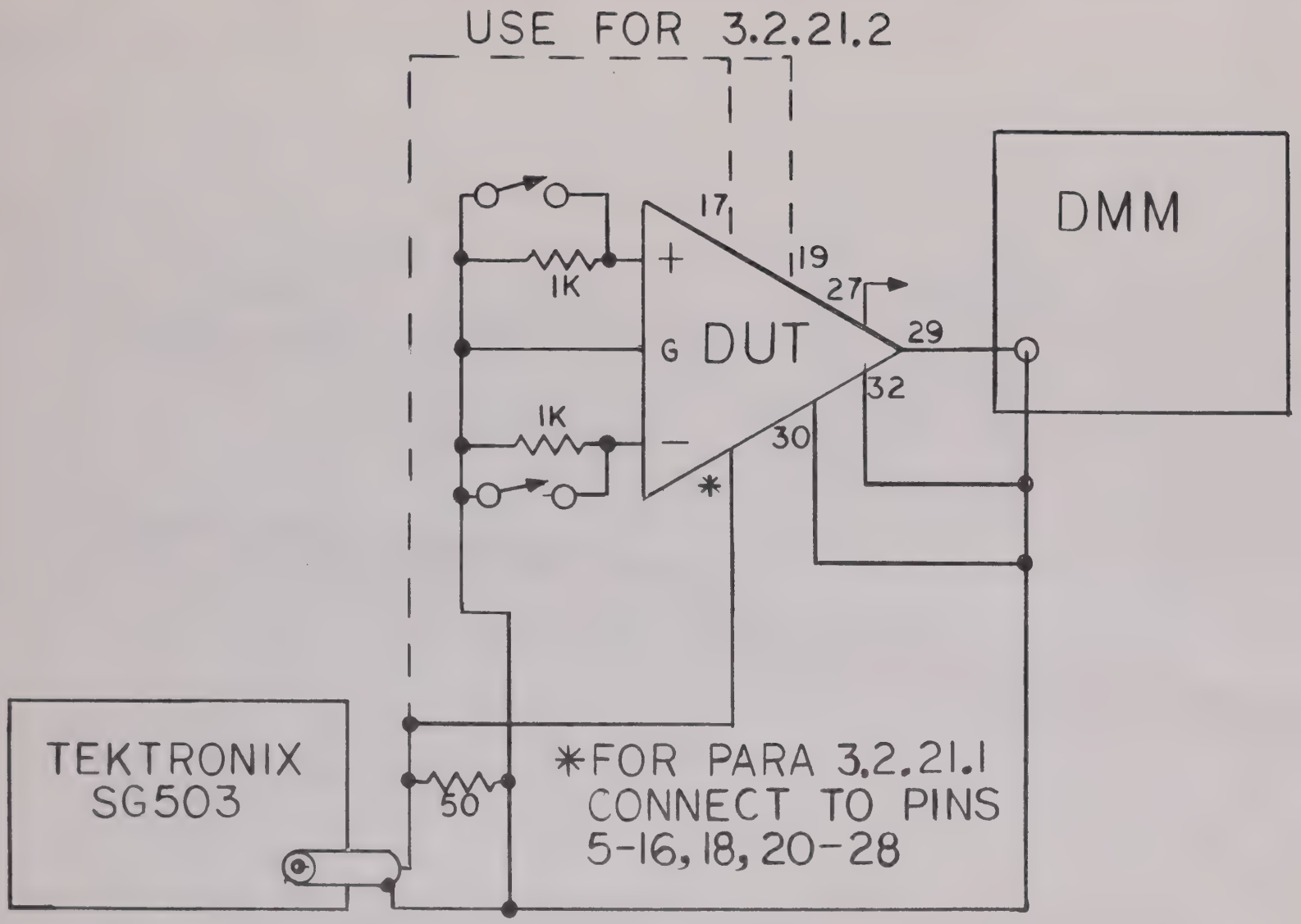
TEST CONNECTIONS
3.21 OVERLOAD INDICATION

FIGURE 10



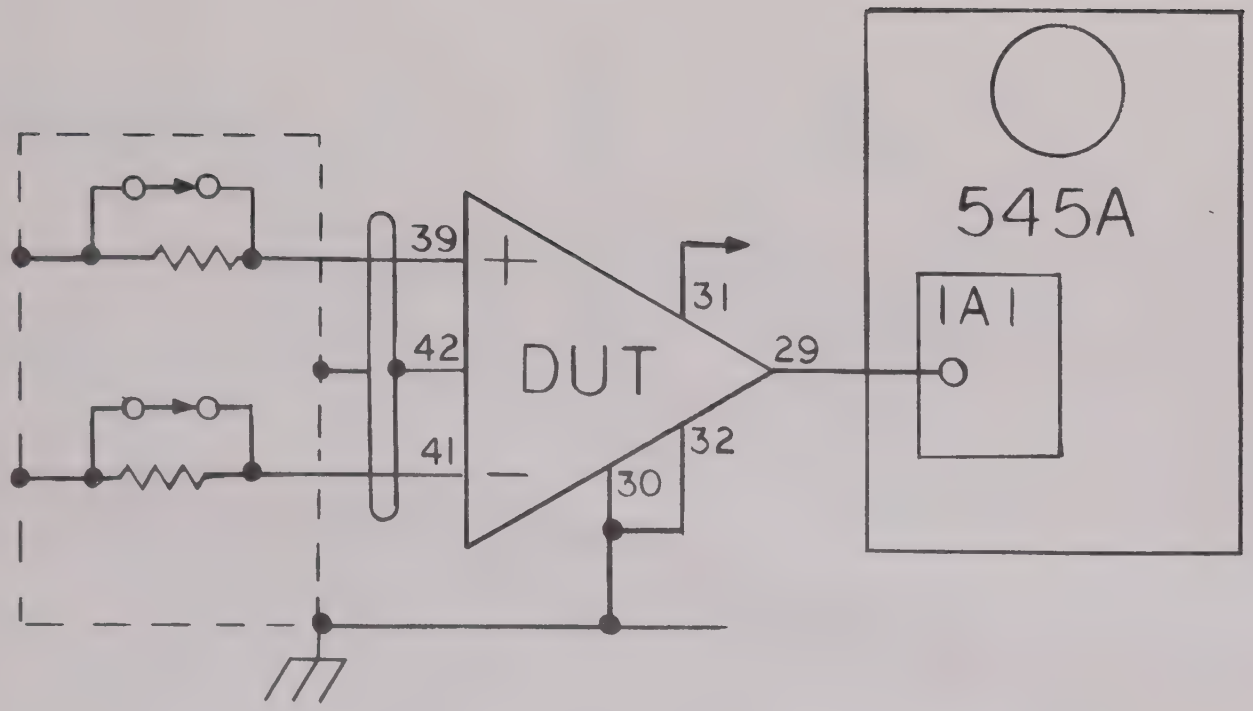
TEST CONNECTIONS
3.25 NOISE SUSCEPTIBILITY

FIGURE 11



TEST CONNECTIONS
3.25 NOISE SUSCEPTIBILITY

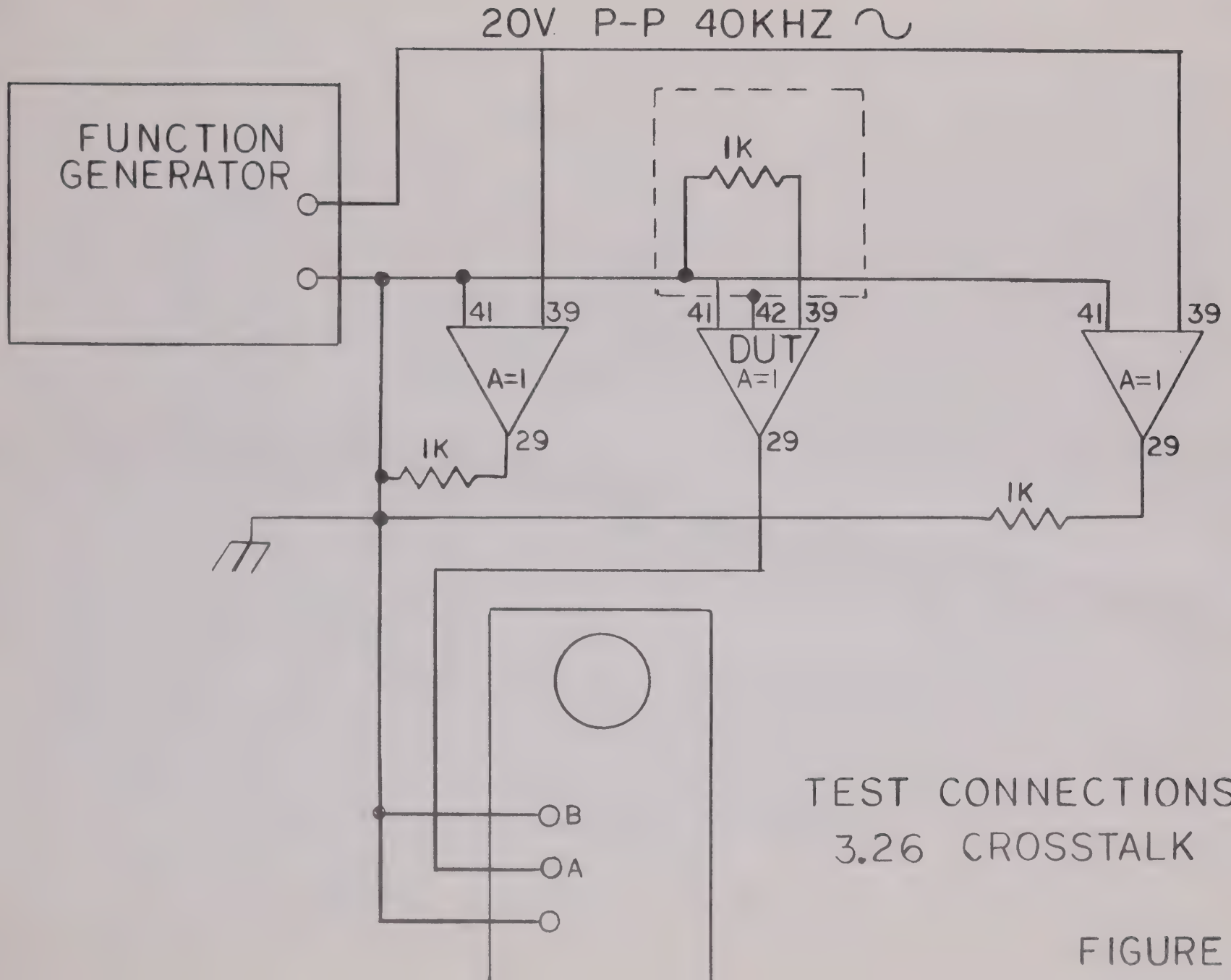
FIGURE 11



TEST CONNECTIONS

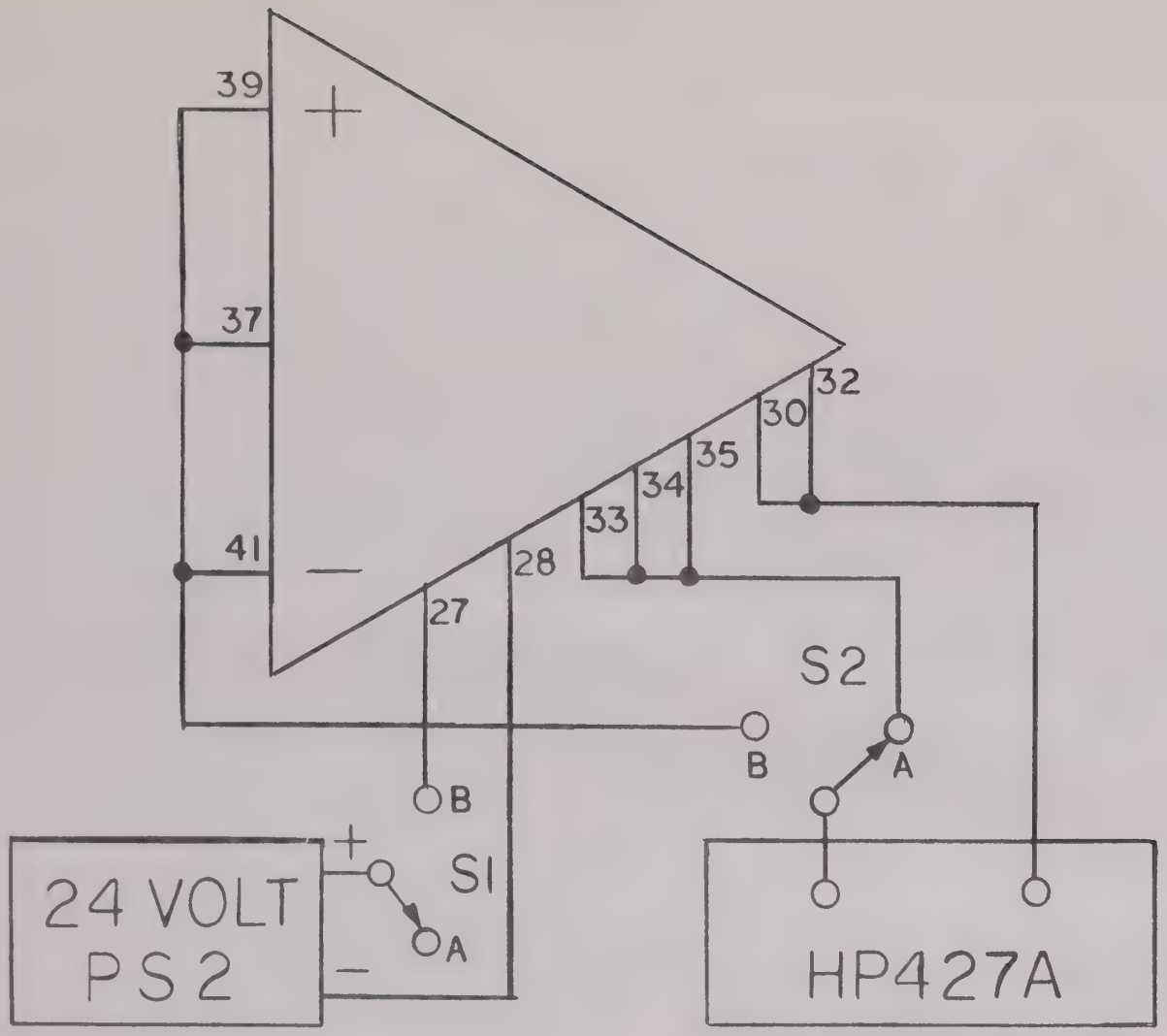
3.23 NOISE

FIGURE 12



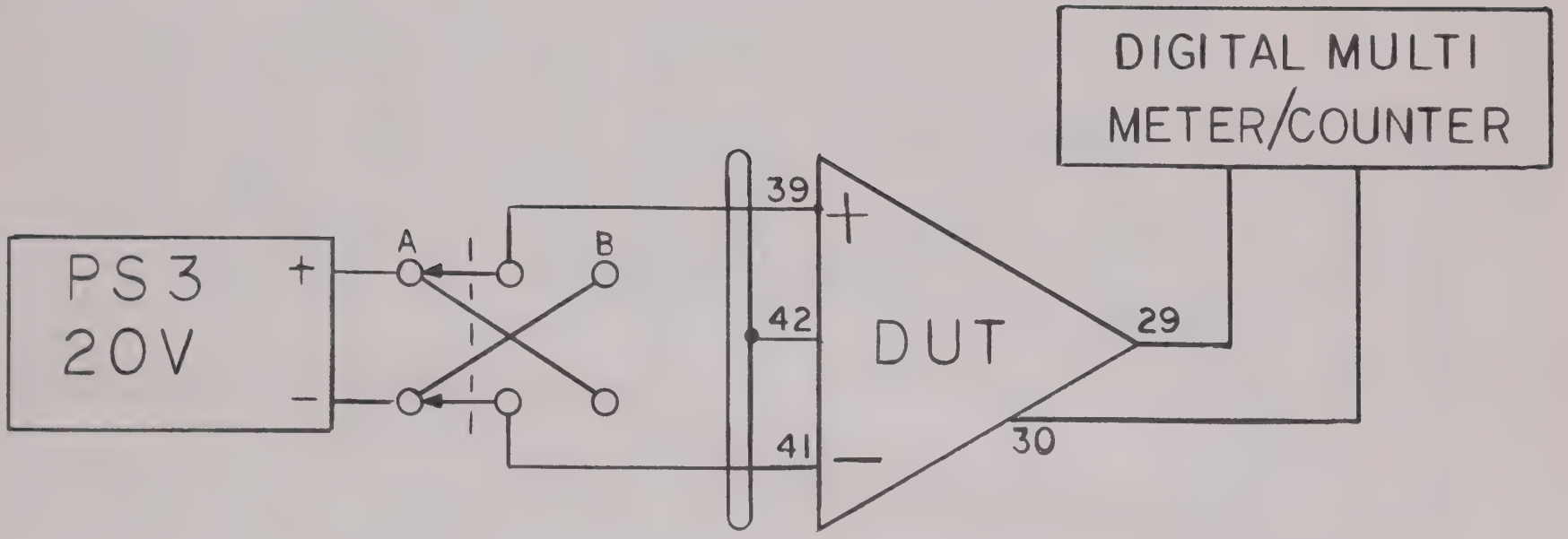
TEST CONNECTIONS
3.26 CROSSTALK

FIGURE 13



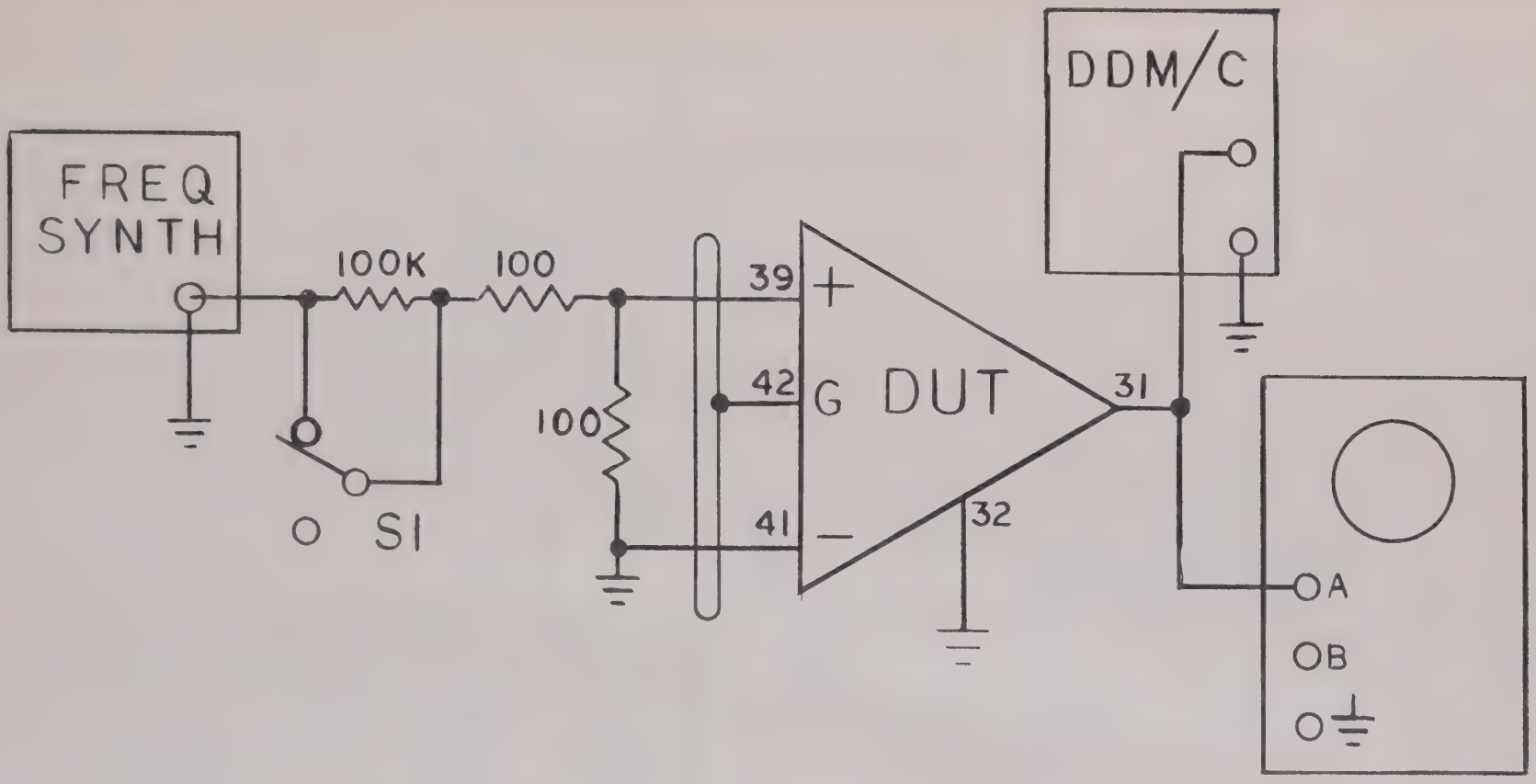
3.13 TEST CONNECTIONS
INPUT ISOLATION

FIGURE 14



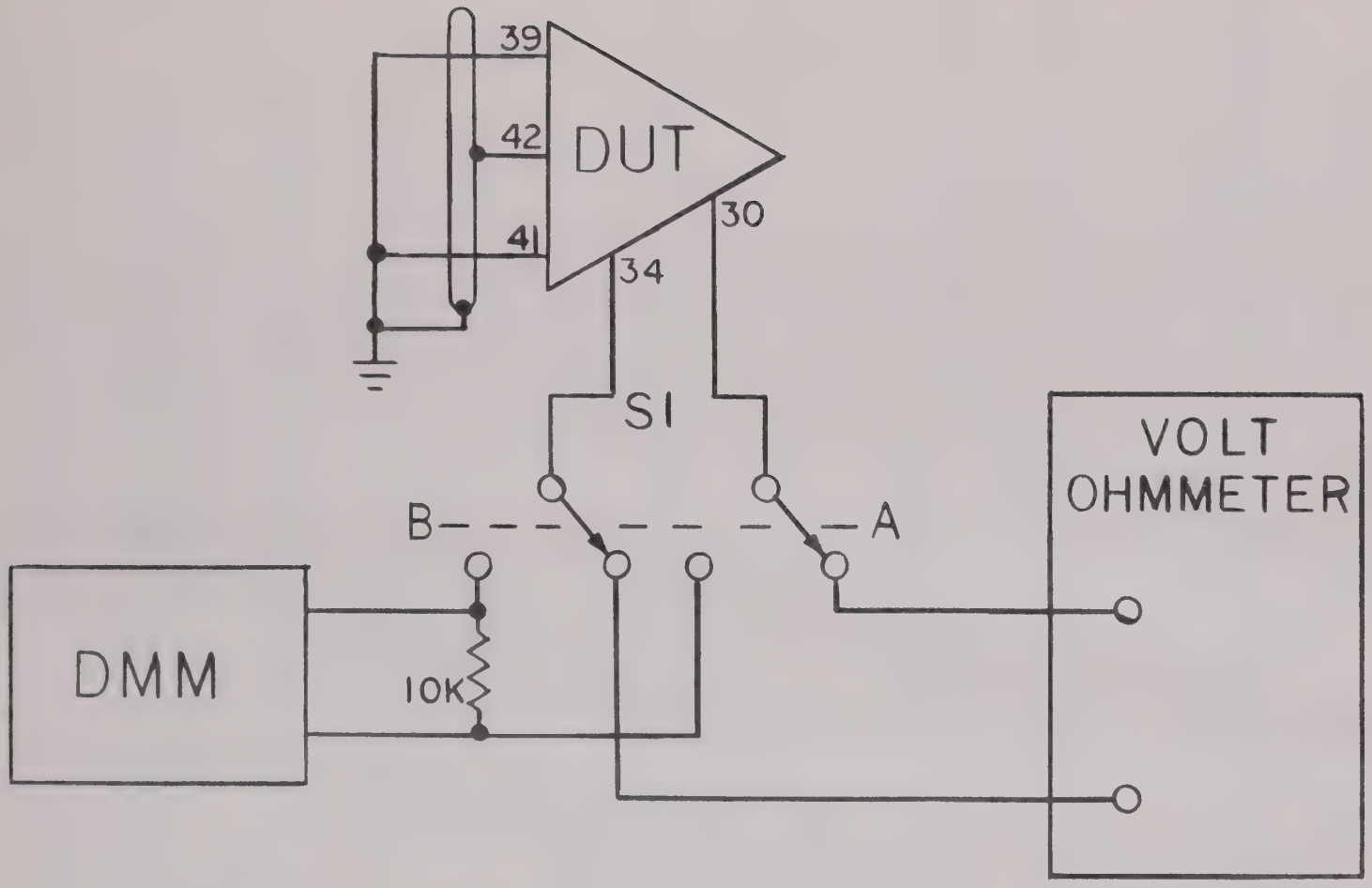
3.1 PLUS AND MINUS 20V
INPUT OVERLOAD

FIGURE 15



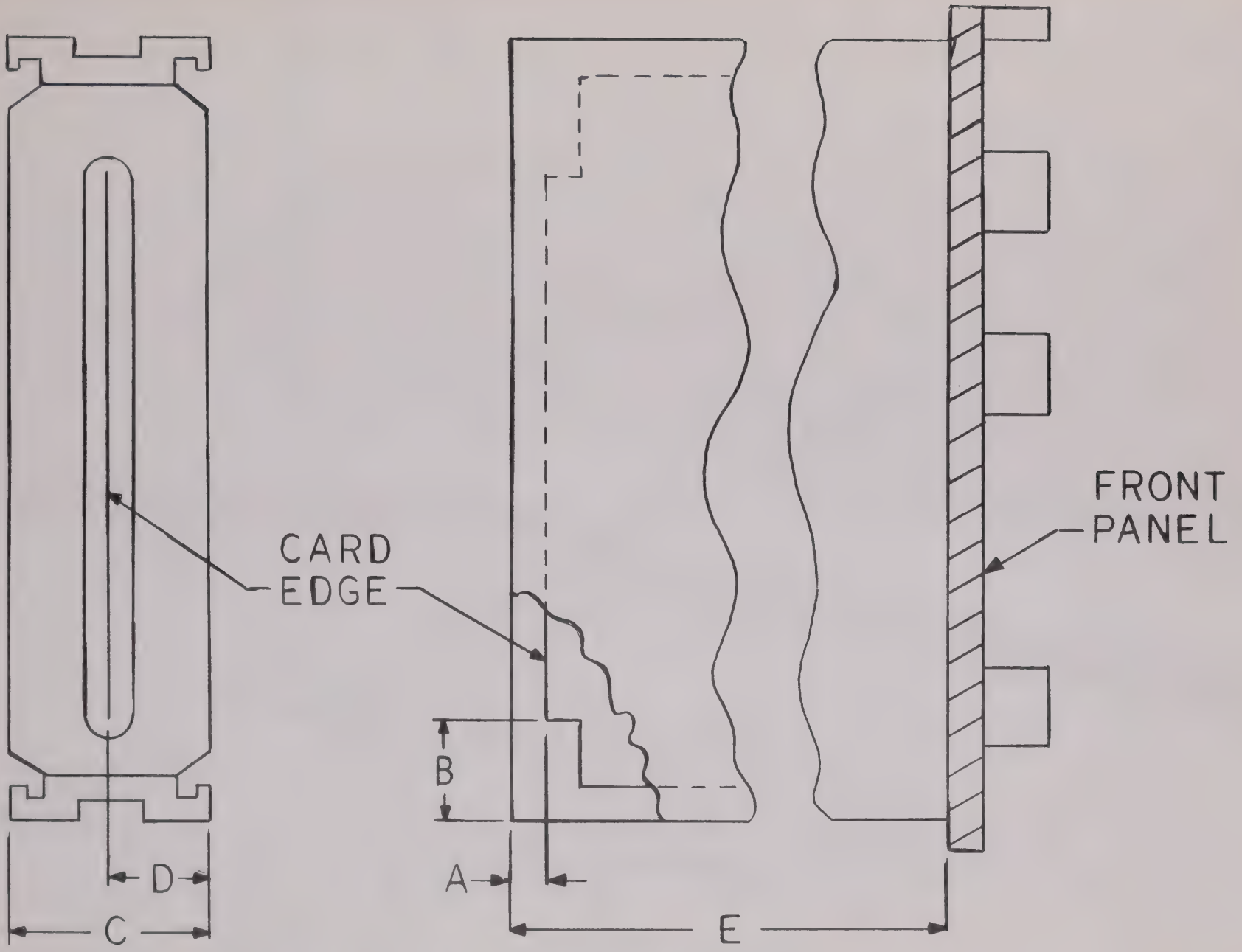
3.5.1 FILTER RESPONSE (>100 HZ)

FIGURE 16



3.31 OUTPUT GUARDING

FIGURE 17



3.32 MECHANICAL DIMENSIONS

FIGURE 18

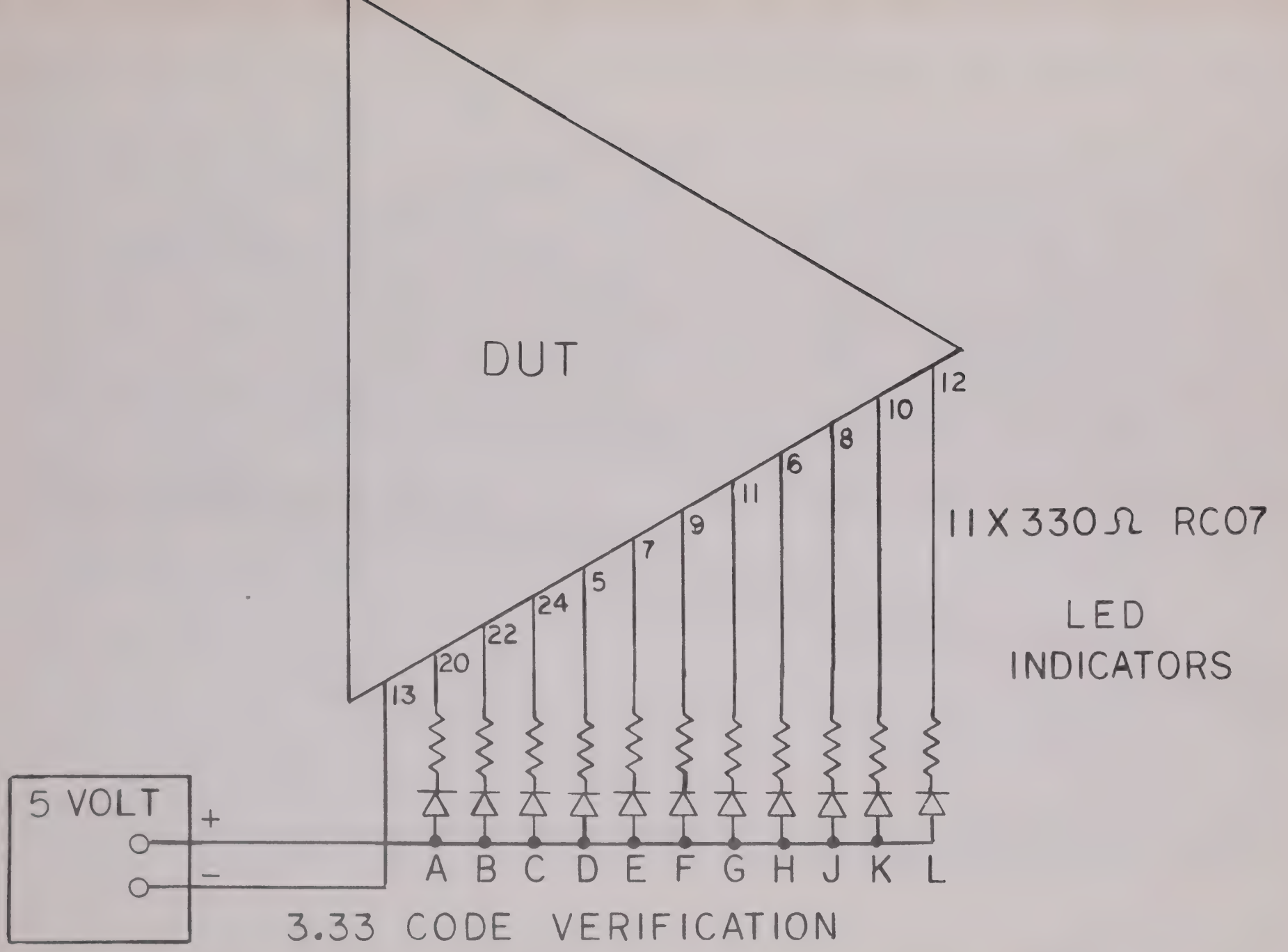
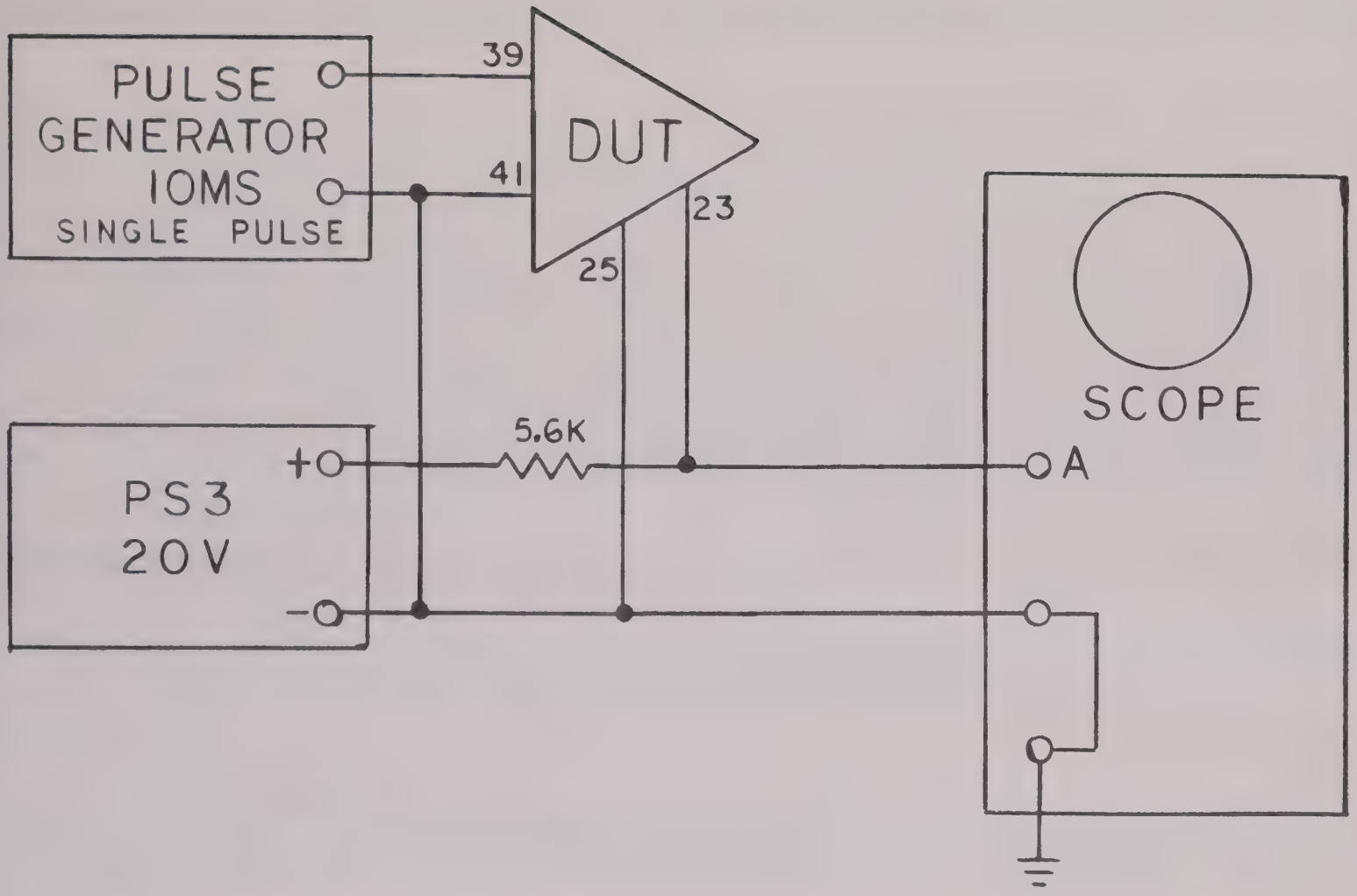

DUT
12
10
8
6
11
9
7
5
24
22
20
13
11 X 330 Ω RC07
LED
INDICATORS
5 VOLT
+
–
A B C D E F G H J K L
3.33 CODE VERIFICATION

FIGURE 19



3.21.16 SHORT DURATION OVERLOAD INDICATION

FIGURE 20

WARRANTY

All Ectron instruments are warranted against defects in material and workmanship for a period of one year from date of shipment to the original purchaser. Ectron agrees to repair or replace any assembly or component (except expendable items such as fuses, lamps and batteries) found to be defective during this period. Ectron's obligation under this warranty is limited solely to repairing or replacing at its option any instrument which in Ectron's sole opinion proves to be defective within the scope of the warranty and when returned to the factory or to an authorized service center. Transportation to the factory or service center is to be prepaid by purchaser. Shipment should not be made without prior authorization by Ectron. This warranty does not apply to products repaired or altered by persons not authorized by Ectron, or not in accordance with instructions furnished by Ectron. If the instrument is defective as a result of misuse, improper repair, alteration, neglect, or abnormal conditions of operation, repairs will be billed at Ectron's normal rates. Ectron assumes no liability for secondary charges or consequential damages as a result of any alleged breach of this warranty, and, in any event, Ectron's liability for breach of warranty under any contract or otherwise shall not exceed the purchase price of the specific instrument shipped and against which a claim is made. This warranty is in lieu of all other warranties, expressed or implied, and no representative or person is authorized to represent or assume for Ectron any liability in connection with the sale of our products other than set forth herein.

PROCEDURE FOR SERVICE

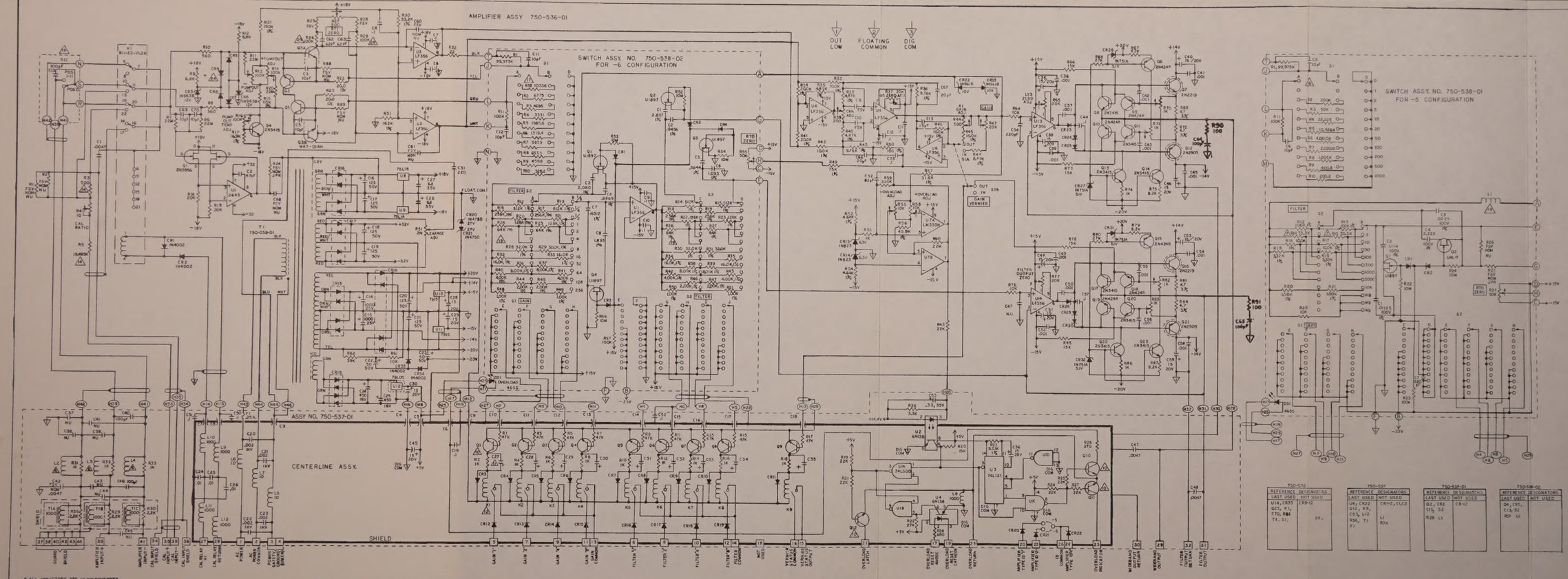
If a fault develops, notify ECTRON or its local representative, giving full details of the difficulty, and including the model number and serial number. On receipt of this information, service data or shipping instructions will be furnished. If shipment is indicated, forward the instrument freight prepaid to the factory or to the authorized service center indicated in the instructions.

DAMAGE IN TRANSIT

The instrument should be tested as soon as it is received. If it is damaged in any way, a claim should be filed with the carrier. A full report of the damage should be obtained by the claim agent, and this report should be forwarded to us. ECTRON will advise the disposition to be made of the equipment and arrange for repair or replacement. Please include model number and serial number in all correspondence referring to the instrument.

(714) 278-0600
TWX 910-335-1259

ECTRON CORPORATION
8159 Engineer Road
San Diego, Ca. 92111



REVISION			
LTR	DESCRIPTION	BY	DATE APP'D
A	INC ECO 276, 277	A.P.	3-7-66
B	INC ECO 376	J.P.	3-30-66
C	INC ECO 814	J.P.	4-11-66

750-536	
REFERENCE DESIGNATIONS	
LAST USED	NOT USED
U14, CR35	CR9-12
Q25, K5, CTO, RB1 T1, S1,	C4,

750-537	
REFERENCE DESIGNATIONS	
LAST USED	NOT USED
U4, CR22	
Q10, R9,	CR1-2, C1, C2
C5, L12	L1
R36, T1	R34
F1	

750-538-01	
REFERENCE DESIGNATIONS	
LAST USED	NOT USED
Q2, CR2	CR1-2
C13, S2	
R28 L1	

750-538-02	
REFERENCE DESIGNATIONS	
LAST USED	NOT USED
Q4, CR5,	
C13, S2	
R54 U1	

NOTE: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE IN OHMS, 5% ¼W.
2. ALL CAPACITORS ARE IN MICROFARADS.
3. ALL DIODES ARE IN4148.
4. ABBREVIATIONS:
   FDV-FACTORY SELECTED VALUE
   NU-NOT USED
5. ALL INDUCTORS ARE IN MICROHENRIES.

6. ALL RELAYS SHOWN IN DE-ENERGIZED POSITION.
7. C3 THRU 18 OF 750-537-01 ARE .001 μF FEED-THRU CAPACITORS.
8. C23,44 ARE ECTRON P/N 026-0001-00.
9. ALL BRIDGE RECTIFIERS ARE 1N0075-0.

△1 BIC LOCATED ON ASSY NO. 750-538-01 & 750-538-02.
△2 R3 & R5 OF 750-536 ARE IN RESISTOR SET 750-033-01.
△3 CR1 THRU R9 OF 750-537-01 ASSY. ARE IN4-600000-00.
△4 C27 THRU C35 OF 750-537-01 ASSY. ARE 1/5/20V.
△5 Q1 THRU Q9 OF 750-537-01 ASSY. ARE 2N3414 OR 2N3415
△6 R14 & 15 OF 750-538-01 ASSY. ARE ECTRON P/N 026-0001-00.
△7 L2,3,4 ARE ECTRON P/N 750-036-01.
△8 R26 & R29 ARE PART OF RESISTOR SET 750-052.
△9 C45, C51, C87-8 ARE ECTRON 1/N032-001-00.
△10 R1-R11 AND R58 OF 750-538-02 ARE IN RESISTOR SET 750-039-01.
△11 R1 THROUGH R11 OF 750-538-01 ARE IN RESISTOR SET 750-054-01.
△12 R42 THROUGH R51 OF 750-538-02 ARE IN RESISTOR SET 750-042-01.
△13 L1 COMPOSED OF FERRITE BEAD ECTRON PART NO. 1-308015-0.

□ INDICATES REAR CARD EDGE CONNECTION.
.XXX INDICATES FRONT PANEL CONTROL.
(1) INDICATES INTERNAL CONNECTION TO 750-537-01 ASSY.
(2) INDICATES INTERNAL CONNECTION TO 750 538-01 OR -02.

| | | |

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CORPORATION

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